EK-DMR11-TM-002

DMR11 synchronous controller technical manual

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PREFACE

This manual describes in detail the installation requirements, programming considerations, and servicing procedures, including diagnostic support, for the DMR11 Synchronous Controller. A variety of appendices are also provided to supplement the above.

Other publications which support the DMR11 Synchronous Controller are:

- *M8207 Microprocessor Technical Manual* (EK-M8207-TM-001)
- *M8203 Line Unit Technical Manual* (EK-M8203-TM-001)
- *DMR11 Print Set* (MP-00911)
- Electronic Industries Association (EIA) Specifications

CHAPTER 1
INTRODUCTION

1.1 SCOPE

This chapter contains a brief introduction to DMR11 operation. The term DMR11, as used throughout this manual, denotes the communication subsystem which consists of a microprocessor module and a line unit module.

1.2 DMR11 GENERAL DESCRIPTION

The DMR11 is designed to be used in a network link for high performance interconnection of VAX-11/780 or PDP-11 computers. It is a microprocessor-based, intelligent synchronous communications controller which employs the DIGITAL Data Communications Message Protocol (DDCMP). The DMR11 is program compatible with DMC11 and line compatible with either DMC11 or any device that uses DDCMP version 4.0.

Features of the DMR11 include:

- Extensive error reporting,
- Down-line and remote load detect to attended or unattended PDP-11 processors (requires bootstrap option),
- Modem control,
- Auto-answering capabilities,
- DMC11 program compatibility,
- Switch selection of DMC11 line compatibility mode or DDCMP V4.0 compatibility mode,
- Comprehensive diagnostic tests,
- Support for local or remote, full-duplex or half-duplex configurations,
- 16-bit non-processor request (NPR), direct memory access (DMA) transfers, and
- DDCMP implementation which handles message sequencing and error correction by automatic retransmission.

The DMR11 basic unit consists of the M8207-RA microprocessor and the M8203 line unit. The microprocessor serves as a parallel data interface between the central processor (VAX-11/780 or PDP-11) and the M8203 line unit. This line unit/microprocessor combination permits either remote or local computer applications. (For remote operations, computers are connected through external modems that use common carrier facilities.) See Figure 1-1 for PDP-11 applications and Figure 1-2 for VAX-11/780 applications.

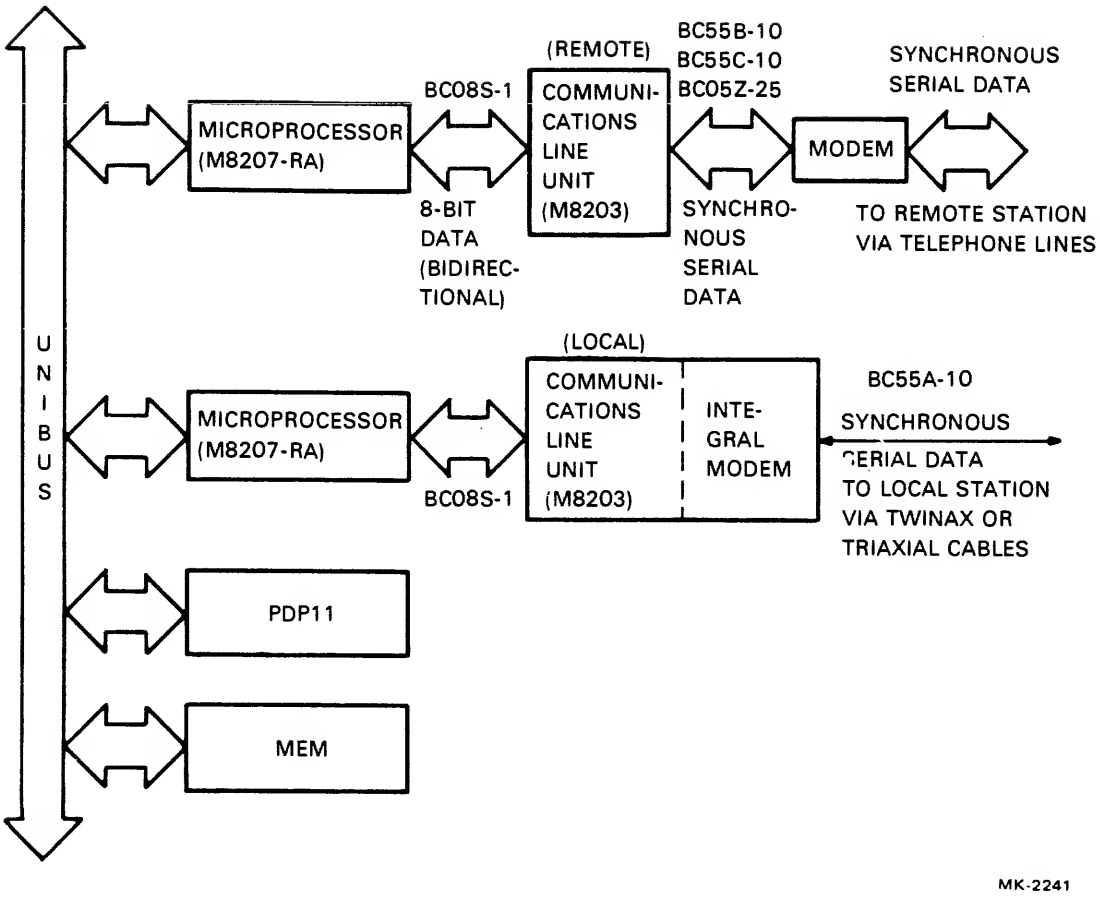


Figure 1-1 Typical PDP-11 Applications

The DMR11 system consists of a basic subsystem and four options which allow it to accommodate standard and special interface configurations. With these options, DMR11 systems can operate with speeds ranging from 2.4K bits per second (b/s) to 1M b/s (see Table 1-1).

Table 1-1 DMR11 Options

Option	Interface	Line Speed
DMR11-AA	EIA RS-232-C* EIA RS-423-A/ CCITT V.10	Up to 19.2K b/s Up to 56K b/s‡
DMR11-AB	ISO 2593/CCITT V.35†	Up to 1M b/s
DMR11-AC	Integral Modem	56K, 250K, 500K, 1M b/s
DMR11-AE	EIA RS-422-A/ CCITT V.11	Up to 1M b/s

*EIA – Electronic Industries Association
†ISO – International Standards Organization
CCITT – Comite Consultatif Internationale de Telegraphic et Telephone
‡Limited to 20K b/s by RS-449 and 9600 b/s by ISO 4902

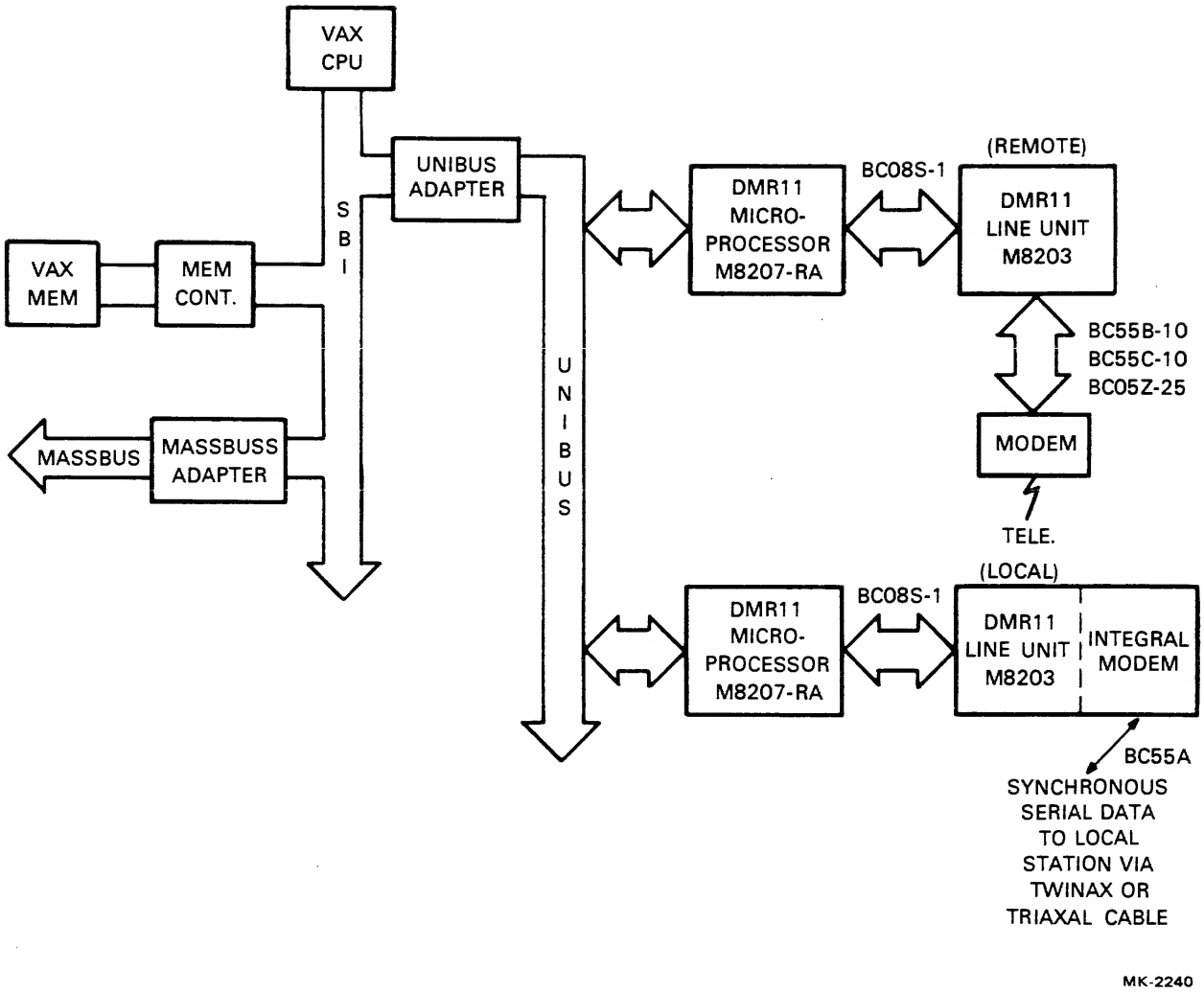


Figure 1-2 Typical VAX-11/780 Applications

The basic subsystem is designated DMR11-AD and consists of an M8203 line unit, an M8207-RA microprocessor, a BC08S-1 interconnect cable, an H3254 interface module test connector, and an H3255 interface module test connector. The M8203 line unit has an Integral Modem which is switch selectable to operate at speeds of 56K, 250K, 500K, and 1M b/s.

For local operations through Integral Modems, systems are interconnected by twinax or triaxial cables in either half-duplex (one cable) or full-duplex (two cables) configurations. The DMR11-AC option is used for local operations. A maximum distance of 6 km (18K feet) at 56K b/s can be obtained using recommended cables. For information on recommended cables, data rates/distance, and fabrication techniques for twinax/triaxial cables, refer to the *M8203 Line Unit Technical Manual,* EK-M8203-TM-001, Appendix B. For specific information on the installation of the DMR11 basic subsystem and its options, refer to Chapter 2.

1.3 DMR11 SYSTEM OPERATION

Operation of the DMR11 is initiated and directed by a user program residing in the central processing unit's (CPU) memory. A user program consists of an application program and a device driver routine

that interfaces with the DMR11. Communication between the user program and the DMR11 is accomplished by four 16-bit control and status registers (CSR) integrated to the microprocessor. These CSRs are used for initializing, selecting the mode of operation, assigning receive or transmit buffers to the DMR11, obtaining receive and transmit buffer returns from the DMR11, and error reporting.

The first two registers in the group have a fixed format and serve as a command header for the second two registers. The second two registers form a two-word data port for the exchange of unique control/status information between the DMR11 and the user program. Data port contents are specified by an identification field in the command header. Other fields in this header control interrupt enabling and status bits for command transfer handshakes between the main CPU and the DMR11.

A user program issues a command to the DMR11 by setting up the input command header and requesting the use of the data port. When the DMR11 grants permission to use the data port, the user program passes the command to the DMR11 in the pertinent CSRs. The DMR11 interprets the command and performs the specified actions.

The DMR11 issues error or status information to the user program by storing the command in the pertinent CSRs and by notifying the user program that the status is available for retrieval and processing.

Message data received or transmitted by the DMR11 is written into or read from the user program assigned buffers in the main CPU memory. The DMR11 accesses these buffers through NPRs to a UNIBUS address. A UNIBUS address is an 18-bit address used by an NPR device to access a device on the UNIBUS or a location in main CPU memory.

1.3.1 Command Structure

As previously stated, communication between the main CPU resident user program and the DMR11 is accomplished through a set of four 16-bit UNIBUS CSRs. This is accomplished by using these CSRs to implement an input and output command structure.

There are five input and three output commands. Their functions are discussed in Chapter 3.

1.3.2 Input Commands

Input commands are issued by the user program to initialize, select the mode of operation, and assign receive or transmit buffers to the DMR11.

1.3.3 Output Commands

Output commands provide a means for the DMR11 to report various normal and abnormal (error) conditions concerning the data transfer operation.

Two basic commands are provided:

1. Receive or Transmit Buffer Address/Character Count Out and
2. Control Out

The Buffer Address/Character Count Out command is used to report a successful, error free completion of a receive or transmit buffer and it indicates the actual number of bytes transferred. This command utilizes both Select 4 (SEL 4) and SEL 6 to identify the address of the completed buffer and the actual character count of the transfer.

The Control Out command is used to report specific conditions concerning the DDCMP, the user program, the hardware, or the modem. Control Out utilizes SEL 6 to inform the user program as to the nature of the report (refer to the following).

- Error Status

  Identifies the reason for the error condition (errors can be associated with the DDCMP, the user program, the modem, or other hardware limitations). In some cases the error condition is non-fatal and normal operations can continue. Other errors are fatal, causing the DMR11 to shut down.

1.3.4 DMR11 Operation Sequencing

The normal sequence of operation is represented in the flow chart in Figure 1-3.

The user program initializes the DMR11 by issuing the Initialize command with the Master Clear bit set. When the DMR11 has completed the initialization, it sets the Run bit. At this point the user program assigns a 128-byte Base Table in CPU memory to the DMR11 for maintaining error counters and storage of vital information on shut-down. This is done using the Base In command. The user program via the Control In command then sets the DMR11 for either half-duplex or full-duplex and either DDCMP Normal or DDCMP Maintenance Mode. If Normal DDCMP Mode is selected, DMR11 initiates protocol start up.

The user program should now assign transmit and receive buffers to the DMR11 via the Buffer Address/Character Count In command. When a transmit buffer is assigned, the DMR11 issues an NPR to retrieve the data from CPU memory for transmission on the serial line.

If there are receive buffers assigned when the DMR11 receives data over the serial line, it issues an NPR to transfer the data to the CPU memory.

The DMR11 performs message sequencing, link management, cyclic redundancy check (CRC) error checking, error connection via retransmission, and some error reporting to the CPU.

1.3.5 Maintenance Mode Operation

A special DDCMP message format, the maintenance message, is used for down-line loading, restarting, or otherwise maintaining satellite computer systems. Messages in this format are subject to error checking but are unsequenced, unacknowledged, and not retransmitted automatically by the microprocessor.

The user program must initialize the DMR11, give it a Base In with the Resume bit clear, and then give a Control In to put the DMR11 in Maintenance Mode.

1.4 GENERAL SPECIFICATIONS

The following paragraphs contain performance, electrical, and environmental specifications for all DMR11 configurations. Table 1-2 lists the performance parameters of the DMR11.

1.4.1 Power Requirements

The M8207-RA and M8203 line unit power requirements are listed below:

Module	Voltage Rating (Approximate Values)
M8207-RA	+ 5 volts @ 5.0 amperes
M8203	+ 5 volts @ 3.0 amperes
	+15 volts @ .11 amperes
	-15 volts @ .2 amperes

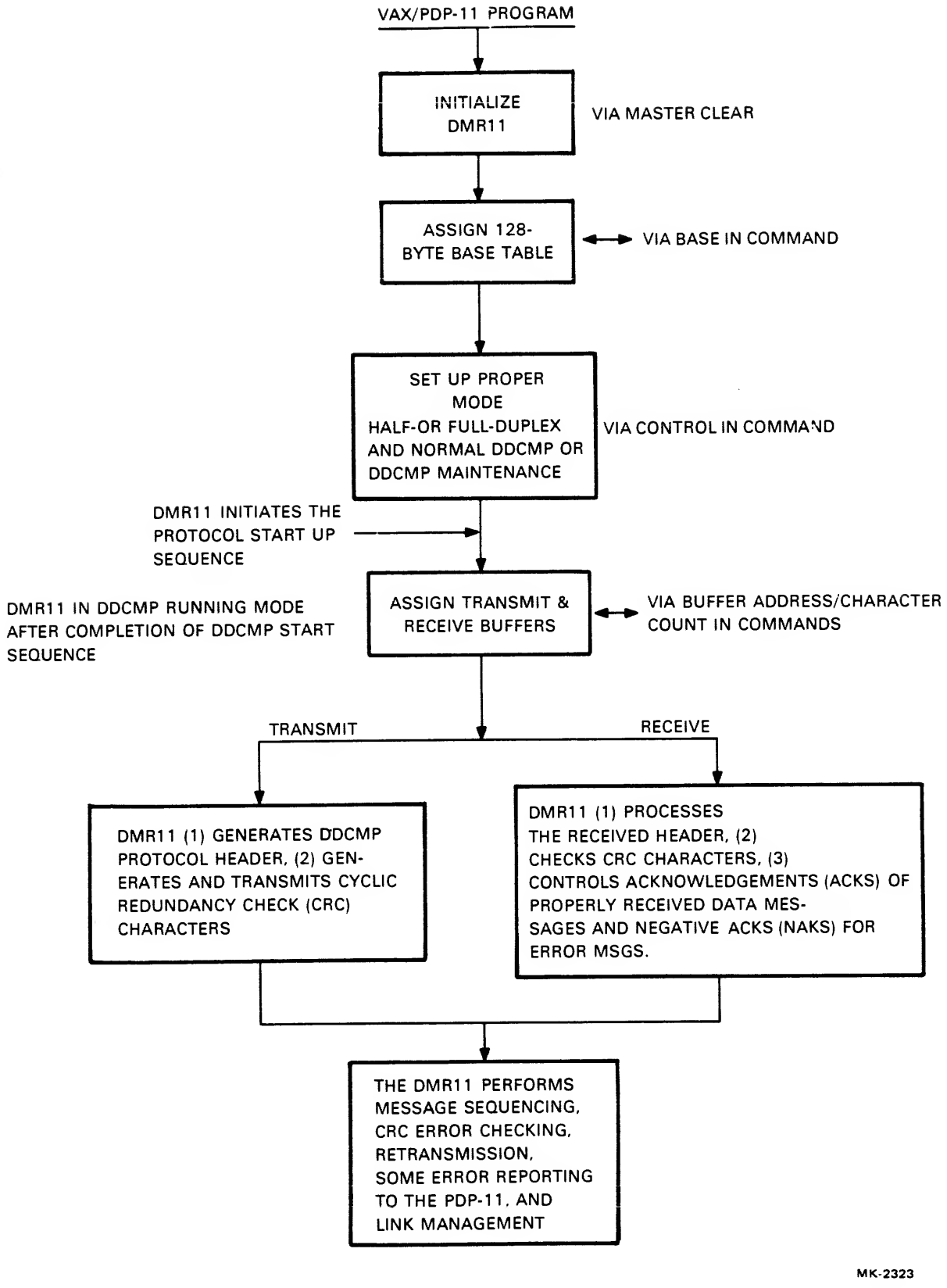


Figure 1-3 DMR11 Operation Sequencing

Table 1-2 DMR11 Performance Parameters

Parameter	Description
Operating Mode	Full-Duplex or Half-Duplex
Data Format	Synchronous DDCMP
Special Data Rates	Up to 1M b/s
Cable Length	Refer to *M8203 Line Unit Technical Manual*, EK-M8203-TM-001, Appendix B

1.4.2 Environmental Requirements - All DMR11s

The DMR11 is designed to operate in a Class C environment as outlined in DEC Standard 102.

- Operating temperature range - 5°C to 50°C (41°F to 120°F)
- Relative humidity - 10 to 90 percent with a maximum wet bulb of 28°C (82°F) and a minimum dewpoint of 2°C (36°F)

1.5 EIA STANDARDS OVERVIEW (RS-449 vs RS-232-C)

The most common interface standard used in recent years has been the RS-232-C. It does, however, have serious limitations for use in modern data communications systems: the most critical being speed and distance.

For this reason, the RS-449 standard has been developed to replace the RS-232-C. It maintains a degree of compatibility with RS-232-C to accommodate an upward transition to RS-449.

The most significant difference between RS-449 and RS-232-C is the electrical characteristics of signals used between the data communication equipment (DCE) and the data terminal equipment (DTE). The RS-232-C standard uses only unbalanced circuits while the RS-449 uses both balanced and unbalanced electrical circuits. The specifications for these different types of electrical circuits supported by RS-449 are contained in EIA Standards RS-422-A for balanced circuits and RS-423-A for unbalanced circuits. These new standards permit much greater transmission speeds and will allow greater distances between the DTE and DCE. The maximum transmission speeds supported by RS-422-A and RS-423-A circuits vary with circuit length; the normal speed limits being 20K b/s for RS-423-A at 200 feet and 2M b/s for RS-422-A at 200 feet. These normal speeds can be exceeded in special applications by trading speed for distance, or vice-versa.

Another major difference between RS-232-C and RS-449 is that two new connectors have been specified to allow for the additional leads needed to support new circuit functions and the balanced interface circuits. One connector is a 37 pin cinch used to accommodate the majority of data communications applications. The other is a nine pin cinch used in applications requiring secondary channel functions. Some of the new circuits that have been added in RS-449 support local and remote loopback testing, and standby channel selection.

The transition from RS-232-C to RS-449 will take some time. Therefore, any applications that are interconnected between RS-232-C and RS-449 must adhere to the limitations of RS-232-C, which has a normal speed of 20K b/s at a maximum distance of 50 feet.

CHAPTER 2
INSTALLATION

2.1 SCOPE

This chapter provides all the necessary information for installing and testing the DMR11 microprocessor subsystem. A checklist, which can be used to verify the installation process, is also included.

2.2 UNPACKING AND INSPECTION

The DMR11 is packaged according to commercial packing practices. When unpacking, remove all packing material and check the equipment against the shipping list (Table 2-1 contains a list of supplied items for each configuration). Inspect all parts and carefully inspect the module for cracks, loose components, and separations in the etched paths. Report damages or shortages to the shipper and notify the DIGITAL representative.

2.3 INSTALLATION CONSIDERATIONS

Installation of the DMR11 microprocessor/line unit subsystem should be done in four phases:

- Phase I - Preinstallation Considerations

  Verify system requirements, system placement, and configuration requirements.

- Phase II - Microprocessor Installation

  Configure, install, and verify microprocessor module via the appropriate diagnostics.

- Phase III - Line Unit Installation

  Configure the line unit module for the customer application and install, cable, and verify it via appropriate diagnostics.

- Phase IV - DMR11 System Testing

  Verify the DMR11 microprocessor subsystem operation with the functional diagnostics and system exercise programs.

2.4 PREINSTALLATION CONSIDERATIONS

The following (Table 2-1) should be considered prior to ordering a DMR11 communications interface to insure that the system can accept the DMR11 and that it can be installed correctly. These steps should also be verified at installation time.

Table 2-1 DMR11 Option Packing List

Option	Parts List	Description
DMR11-AD		DMR11 basic subsystem unit containing:
	M8203	Line unit module
	M8207-RA	Microprocessor module with DMR11 microcode ROMS
	BC08S-1	Module interconnect cable
	H3254	V.35 and integral module test connector
	H3255	RS-232-C/RS-422-A/RS-423-A module test connector
	EK-DMR11-UG-001	*DMR11 User's Guide*
	MP-00911	Customer print set
	ZJ-306-RB	Diagnostic set
DMR11-AA		RS-232-C/RS-423-A interface configuration containing:
	DMR11-AD	Basic DMR11 unit
	BC55C-10	EIA RS-232-C/RS-423-A cable
	H3251	Cable turnaround test connector
	H325	Cable turnaround test connector
DMR11-AB		CCITT V.35 interface configuration containing:
	DMR11-AD	Basic DMR11 unit:
	BC05Z-25	CCITT V.35 cable
	H3250	Cable turnaround test connector
DMR11-AC		Integral Modem interface configuration containing:
	DMR11-AD	Basic DMR11 unit
	BC55A-10	Integral Modem cable
	H3257	BC55A terminators
	H3258	
DMR11-AE		RS-422-A interface configuration containing:
	DMR11-AD	Basic DMR11 unit
	BC55B-10	RS-422-A cable
	H3251	Cable turnaround test connector

2.4.1 System and Device Placement

2.4.1.1 System Placement – On systems that contain many high speed direct memory access (DMA) devices, there is a probability of adverse bus latency. To help prevent this occurance, the closer the

physical placement of the DMR11 to the processor, the higher the DMA device priority. A single DMR11 at 1M b/s and in full-duplex mode is capable of transferring 125,000 bytes/second/channel X 2 channels (Transmit and Receive). Because the DMR11 performs 16-bit word transfers via nonprocessor request (NPR) transactions to memory, approximately 125,000 NPRs per second at the rate of 8 microseconds/NPR are generated. Customer applications using speeds greater than 250K bits per second (b/s) require UNIBUS placement before all UNIBUS repeaters and before all devices that have a lower NPR rate on the UNIBUS.

2.4.1.2 Device Placement – The DMR11 requires two hex-height, small peripheral controller (SPC) backplane slots (preferably two adjacent slots). Any SPC backplane [DD11-B(REV E) or later] can accept the DMR11. The DD11-D can accommodate a maximum configuration of three DMR11s.

CAUTION

Each DMR11 requires approximately 8 amperes from the +5 volt source. Check to ensure that the supply is capable of providing a total of 24 amperes if a maximum configuration is installed.

2.4.2 System Requirements

1. UNIBUS Loading

   M8207-RA microprocessor — 1 UNIBUS dc load, 5 UNIBUS ac loads

   M8203 line unit — No UNIBUS loads

2. Power Requirements

   Check the power supply before and after installation to ensure against overloading. The microprocessor/line unit total current requirement for the +5 volt supply is approximately 8 amperes. Additionally, the unit requires ±15 volts for the silos, level conversion logic, and Integral Modem. Power requirements for the microprocessor/line units are listed in Table 2-2.

Table 2-2 DMR11 Voltage Chart

Module	Voltage Rating (Approximate Values)	Maximum Voltage	Minimum Voltage	Back Plane Pin
M8207-RA	+ 5 Volts @ 5.0 A	+ 5.25	+ 5.0	C1A2
M8203	+ 5 Volts @ 3.0 A	+ 5.25	+ 5.0	C1A2
	+15 Volts @ .1 A	+15.75	+14.25	C1U1
	-15 Volts @ .2 A	-15.75	-14.25	C1B2

3. Interrupt Priority

   The interrupt priority is selected by priority plug E77 on the M8207-RA microprocessor module. This plug is preset to select priority five (BR5). Refer to Figure 2-1 for the priority plug location.

4. Device Address Assignment

   The DMR11 resides in the floating address space of the Input/Output (I/O) page of memory. The ranking assignment of the DMR11 is equal to the DMC11 ranking number seven.

   The selection of the device address is accomplished by Switch Pack E127 on the M8207-RA microprocessor module. Refer to Figure 2-1 for the switch pack placement. Since the DMR11 will reside at the same ranking as the DMC11, the operating system can determine what type of device resides at that address location by reading the second control and status register (CSR) of the device and examining the high byte.

   If the bootstrapping feature of the DMR11 or DMC11 is to be used, only the devices that reside at unit zero and/or unit one address location can implement this feature, unless bootstrap is designed to accept more units.

   Refer to Appendix A if more information is needed on the floating address allocation.

5. Device Vector Address Assignment

   The DMR11 resides in the floating vector space of the reserved vector area of memory. The ranking assignment of the DMR11 is equal to the DMC11 ranking number 27. The selection of the device vector address is accomplished by Switch Pack E28 on the M8207-RA microprocessor module. Refer to Figure 2-1 for the location of the switch pack. Appendix A contains more information on floating vector allocation.

2.5 MICROPROCESSOR INSTALLATION

2.5.1 Backplane Considerations

Perform the following on the SPC slot that will contain the DMR11, M8207-RA microprocessor module (selected at preinstallation).

1. Verify that the backplane voltages are within the specified tolerances listed in Table 2-2.

2. Turn system power off and remove the NPR Grant (NPG) wire that runs between CA1 and CB1 on that backplane slot for the M8207-RA module.

   NOTE
   Be sure to replace this jumper if the microprocessor is removed from the system.

3. Perform resistance checks on the backplane voltage sources to ground to ensure that no short circuit conditions exist. Refer to Table 2-2 for backplane pin assignments.

2.5.2 M8207-RA Considerations

Perform the following on the DMR11 M8207-RA microprocessor module.

1. Ensure that the module version number is an M8207-RA, which indicates DMR11 microcode.

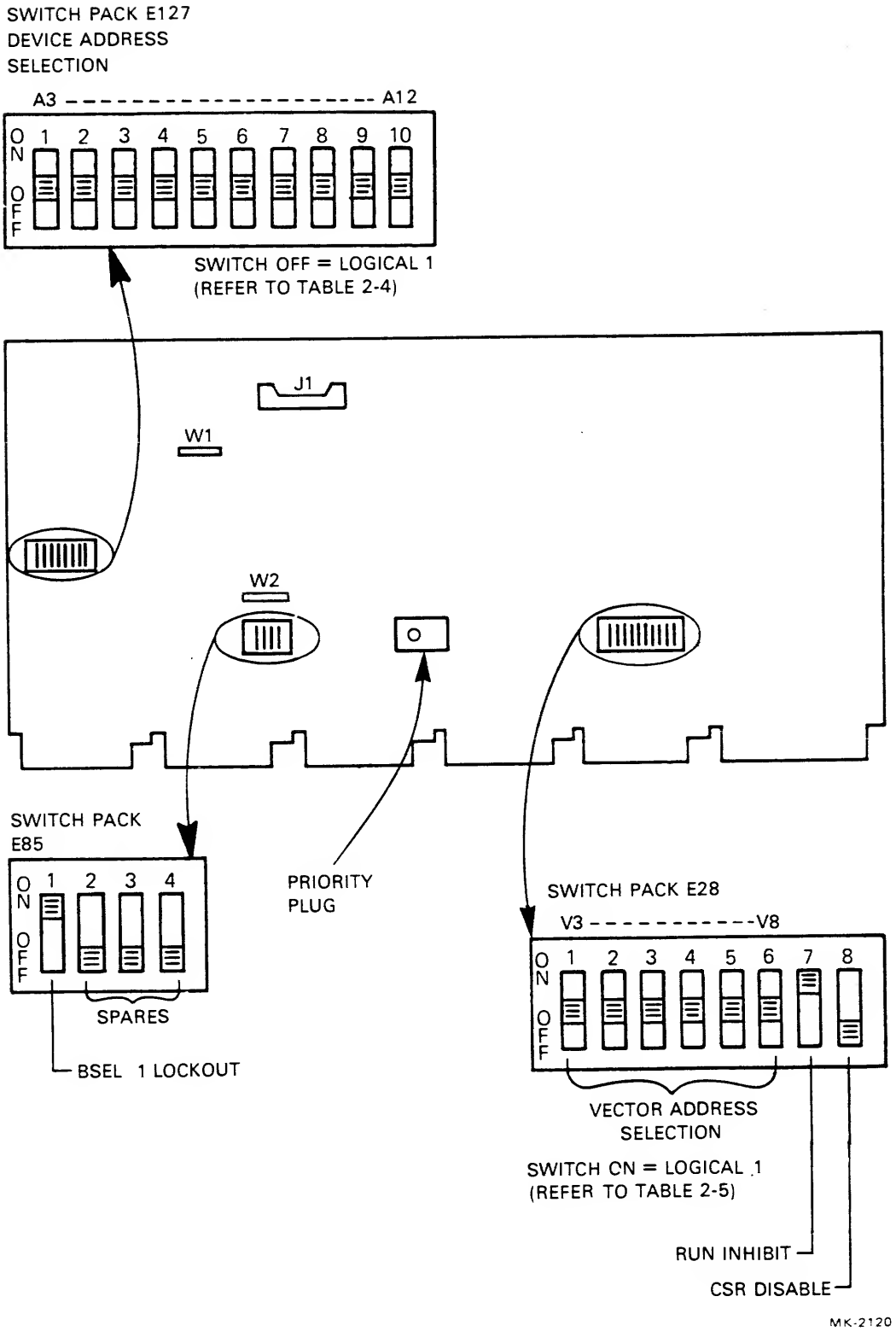


Figure 2-1 M8207-RA Microprocessor Switch/Jumper Locations

2. Verify that M8207-RA jumpers W1 and W2 are installed correctly (refer to Jumper Table 2-3).

3. Configure Switch Pack E127 to implement the correct device address for the DMR11 as determined from the floating address allocation. Refer to Table 2-4 for the correlation between switch number and address bit. A switch OFF (open) responds to logical one on the UNIBUS. Refer to Appendix A for additional information on floating address allocation.

4. Configure Switch Pack E28 to implement the correct vector address for the DMR11 as determined from the floating vector allocation. Refer to Table 2-5 for the correlation between switch number and vector bit. A switch ON (closed) responds to a logical one on the UNIBUS. Refer to Appendix A for additional information on floating vector allocation.

5. Verify that the switch selectable features of the M8207-RA are configured as follows (Table 2-6 provides a summary of switch selectable features):

   - Run Inhibit – Switch Pack E28, switch 7; always ON.
   - CSR Inhibit – Switch Pack E28, switch 8; always OFF.
   - Byte Select/Lockout (BST) – Switch Pack E85, switch 1, normally ON (allows all functions in Byte Select 1 to be used). If the switch is OFF, the Run bit is always asserted and will not allow diagnostic testing.

NOTE
Switch Pack E85, switches 2, 3, and 4 are not used.

6. Verify that the priority plug is a BR5 and is installed correctly in location E77.

Table 2-3 M8207-RA DMR11 Jumper Chart

Jumper Number	Normal Configuration	Function
W1	Always In	Microprocessor Clock Enable – When removed it disables the microprocessor clock. Removed only for automatic module testing at the factory.
W2	Always In	Bus ac Low Enable – When removed it disables a program asserted ac low signal passed onto the UNIBUS.

2.5.3 M8207-RA Insertion

Carefully insert the M8207-RA microprocessor module into the selected SPC slot and perform the following tasks:

1. Perform resistance checks on the backplane voltage sources to ground to ensure that no short circuit conditions exist on the module. Refer to Table 2-2 for backplane pin assignments.

2. Turn system power ON and verify that the backplane voltages are within the specified tolerances listed in Table 2-2.

3. Load and execute the M8207 static diagnostics, parts one and two (no test connectors are required).

   A. PDP-11 System

      CZDMP* M8207 Static Test 1
      CZDMQ* M8207 Static Test 2

   B. VAX-11/780 Systems

      EVDXA COMM Microprocessor Repair Level Diagnostics
      REV *.*

   Chapter 4 provides additional information on these diagnostics. Upon obtaining a minimum of five error free end passes, proceed to the M8203 line unit installation section.

2.6 LINE UNIT INSTALLATION

The M8203 line unit is a universal module with various types of interface capabilities. The M8203 line unit does not present any ac or dc loads to the UNIBUS and only draws power from the backplane slot in which it resides. All data and control signals flow into and out of the line unit via a berg port to the microprocessor. Because of the various M8203 applications, the configurations for each may be different and are selected via switches, jumpers, and different cables. To provide a better understanding of these variations, a number of tables describing each switch pack, jumper, and cable function (as listed below) has been created for reference. Table 2-7 lists the normal M8203 line unit configurations for the different types of DMR11 options without the bootstrap feature selected. Also, refer to the following:

- Table 2-8 Jumper Functions – These jumpers are used to select various interface standard parameters and modem interface signals, depending on application and modem type. Additional jumpers are available on the BC55C (panel) cable for additional interface signal selection.
- Table 2-9 Switch Pack E39 Functions – This switch pack allows proper selection of interface driver and receiver control logic and different line speeds for various applications.
- Table 2-10 Switch Pack E121 Functions – This switch pack is provided for the selection of the bootstrap offset address for the remote load detect feature (if used) and for various microcode switch features.
- Table 2-11 Switch Pack E134 Functions – This switch pack is provided for the selection of the bootstrap password for the remote load detect feature (if used) and for various microcode switch features.
- Table 2-12 Cable Description – This table lists the functions and uses of each cable used with the DMR11.
- Figure 2-2 shows the jumper and switch pack placements on the M8203 line unit.
- Figure 2-3 shows the microprocessor and line unit installation.
- Figure 2-4 shows the outline drawings of DMR11 cables.

Table 2-4 Switch Pack E127 Selections

Switches	Function
1-10	Device Address Selection:

MSB LSB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	SWITCH PACK E127										0	0	0

SWITCH NUMBER	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	DEVICE ADDRESS
										OFF	760010
									OFF		760020
									OFF	OFF	760030
								OFF			760040
								OFF		OFF	760050
								OFF	OFF		760060
								OFF	OFF	OFF	760070
							OFF				760100

						OFF					760200

						OFF	OFF				760300

					OFF						760400

					OFF		OFF				760500

					OFF	OFF					760600

					OFF	OFF	OFF				760700

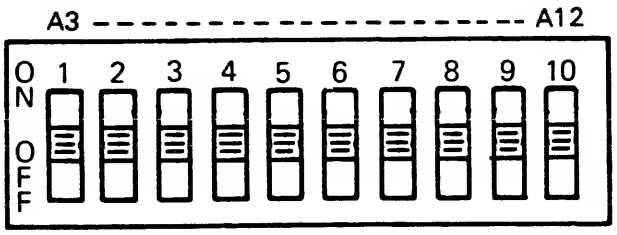
				OFF							761000

			OFF								762000

			OFF	OFF							763000
											--
		OFF									764000

NOTE: SWITCH OFF RESPONDS TO LOGICAL ONE ON THE UNIBUS.

SWITCH PACK E127
DEVICE ADDRESS
SELECTION



Switch Pack E127

Table 2-5 Switch Pack E28 Selections

Switches	Function
	NOTE **Switch ON equals a logical one (1) on the UNIBUS.**
1-6	Vector Address Selection:

MSB **LSB**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	SWITCH PACK E28						1/0	0	0

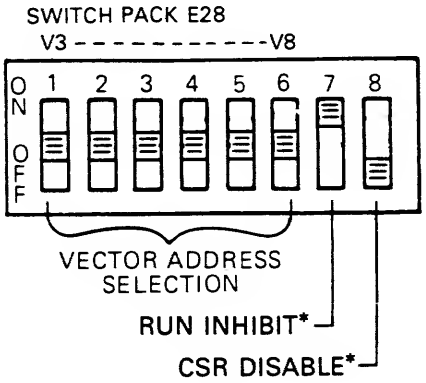
SWITCH NUMBER	S6	S5	S4	S3	S2	S1	VECTOR ADDRESS
		ON	ON				300
		ON	ON			ON	310
		ON	ON		ON		320
		ON	ON		ON	ON	330
		ON	ON	ON			340
		ON	ON	ON		ON	350
		ON	ON	ON	ON		360
		ON	ON	ON	ON	ON	370
	ON						400

	ON		ON				500

	ON	ON					600

	ON	ON	ON				700

NOTE: SWITCH ON PRODUCES LOGICAL ONE ON THE UNIBUS.



*Refer to Table 2-6 for switch functions.

Table 2-6 Switch Selectable Features

Switch Location and Number	Normal Configuration	Function
E28 Switch 7	ON	Run Inhibit - Under normal conditions, switch ON. The initialization of the microprocessor directly sets the run flip-flop which allows the microcode to be executed immediately. Because of an internal malfunction or execution of erroneous microcode during power up, it is possible for the microprocessor to hang the UNIBUS. Placing the Run Inhibit switch in the OFF position clears the Run flip-flop and allows the diagnostics to be loaded to determine the fault. Once diagnostics have been executed and the problem corrected, return the Run switch to the ON position.
E28 Switch 8	OFF	CSR Inhibit - When the switch is ON it keeps the device from responding to its address. Used in special applications on other options.
E85 Switch 1	ON	BSEL 1 Lockout (BST) - When the switch is OFF, it inhibits the use of all maintenance test features and keeps the Run bit asserted at all times. This allows the DMR11 microcode to run with the ability to detect a boot request message at all times. This is used at unattended computer sites. This switch must be ON to execute all diagnostics. **NOTE** **Although BSEL 1 Maintenance functions are inhibited, Master Clear (bit 6) is still functional.**
E85 Switches 2, 3, and 4	OFF	Not Used

Table 2-7 Normal M8203 Configuration (Bootstrap Not Selected)

M8203 Configuration	Option Type:	DMR11-AA EIA RS-232-C or RS-423-A	DMR11-AB CCITT V.35	DMR11-AE EIA RS-422-A	DMR11-AC Integral Modem 56K b/s	DMR11-AC Integral Modem 1 MEG b/s	DMR11-AA Null Modem Clock 9.6K b/s
Jumper Configuration* (refer to Table 2-8)	W1-W6, W11 W14-W17	OUT	OUT	OUT	OUT	OUT	OUT
	W7-W10 W12,W13	IN	IN	IN	IN	IN	IN
Switch Pack E39 (refer to Table 2-9)	S1-4	OFF	OFF	OFF	OFF	OFF	OFF
	S5	OFF	ON	OFF	OFF	OFF	OFF
	S6	OFF	OFF	OFF	OFF	OFF	OFF
	S7	OFF	OFF	ON	OFF	OFF	OFF
	S8	ON	ON	ON	OFF	ON	OFF
	S9	ON	ON	ON	OFF	ON	ON
	S10	OFF	OFF	OFF	ON	ON	OFF
Switch Pack E121 † (refer to Table 2-10)	S1-8	ON	ON	ON	ON	ON	ON
	S9	OFF	DMR11 to DMC11-AL	OFF	DMR11 to DMC11-AR	ON	DMR11 to DMR11 @ 1M b/s	ON	DMR11 to DMR11
	S10	OFF		ON		OFF		ON	
Switch Pack E134† (refer to Table 2-11)	S1-8	OFF	OFF	OFF	OFF	OFF	OFF
	S9	OFF	OFF	OFF	OFF	OFF	OFF
	S10	ON = Disables Microdiagnostics At Master Clear Time OFF = Enables Microdiagnostics At Master Clear Time NOTE: Switch selections for BSEL 1, Bit 13 = 0 at Master Clear Time.					
Cables Required (refer to Figure 2-4)		BC55C-10* and BC05D-25	BC05Z-25	BC55B-10 and BC55D-33	BC55A-10 and Twinax Cables	BC55A-10 and Triax Cables	BC55C-10* and Null Modem
Module Turnaround Test Connector (refer to Figure 2-5)		H3255 IN J2	H3254 IN J1	H3255 IN J2	H3254 IN J1	H3254 IN J1	H3254 IN J2
Cable Turnaround Test Connector (refer to Figure 2-5)		EIA RS-232-C H325	H3250	H3251	Half-duplex Switch ON and Cables Removed	Half-duplex Switch ON and Cables Removed	EIA RS-232-C H325
		EIA RS-423-A H3251					EIA RS-423-A H3251

*Modem variable
† Customer application variable

Table 2-8 M8203 Jumper Functions

Jumper	Normal Configuration	Function
W1	OUT	Clear to Send EIA/V.35
W2	OUT	Data Mode EIA/V.35
W3	OUT	Receive Data EIA
W4	OUT	Receive Clock EIA
W5	OUT	Receive Ready EIA
W6	OUT	Transmit Clock EIA
W7	IN	Signal Rate Indicate – When removed, opens signal to interface in RS-422-A and RS-232-C configurations. Remove when an BC05C-XX* cable is used as this signal is presented to cinch pin nine, which has a positive test voltage on some modems.
W8	IN	Data Mode (Data Set Ready) – When removed, opens signal to interface in RS-422-A/423-A configurations. It has no effect in RS-232-C. Remove when a BC05C-XX* cable is used, as the signal is presented to cinch pin 18, which is dibit clock on some modems.
W9	IN	Null Modem Clock – When removed the signal amplitude is lowered below the interface standards so as not to create interference in some modems.
W10	IN	Terminal Ready – When removed, it opens the signal to modem in RS-422-A/423-A configurations. Remove when a BC05C-XX* cable is used, as this signal is presented to cinch pin 10, which is negative test voltage on some modems.
W11	OUT	Receiver Ready (Carrier Detect) – When installed, it allows this signal to be on at all times. This could cause a problem with the microcode since the Universal Synchronous Receiver/Transmitter (USYRT) will be enabled all the time.
W12	IN	Terminal in Service (Make Busy) – When removed, it opens this signal to the modem. Some modems will not answer the phone and will be put in Analog Loopback when this signal is asserted. When a BC05C-XX* cable is used, this signal is presented at cinch pin 25.

*DMR11 does not support the use of a BC05C-XX cable.

Table 2-8 M8203 Jumper Functions (Cont)

Jumper	Normal Configuration	Function
W13	IN	Oscillator Enable – To be removed only for factory automatic testing. Jumper should always be installed in the field.
W14 and W15	OUT OUT	56K Bandpass Filter Enable – With these jumpers installed, the bandpass filter is limited to 56K b/s. Used in special applications only.
W16	OUT	Switched RTS-CTS Enable – When this jumper is installed, it enables the request to send and clear to send interlock in the M8203 line unit which inhibits asserting RTS, until CTS is dropped. This jumper should never be installed when the DMR11 is operating with a modem that has the constant CTS option installed.
W17	OUT	Half-Duplex Lockout Enable – When this jumper is installed, it enables the M8203 line unit half-duplex lockout feature when half-duplex mode is selected. The lockout feature disables the transmitter or receiver when the other is active. This jumper applies only to half-duplex applications. It must not be installed for full-duplex applications.
		NOTE **Jumpers W16 and W17 are mutually exclusive. Only one or the other may be installed, not both. Also, these jumpers are provided only on M8203 modules REV E or higher. For modules up to REV D, refer to ECO-M8203-MK-007 for details of similar jumpers.**

*DMR11 does not support the use of a BC05C-XX cable.

Table 2-9 Switch Pack E39 (Z) Selections

Switches	Function
	NOTE **Switch off equals a logical one (1).**
1-4	Not used in DMR11.
5-7	Interface Selection – Selects proper drivers and receivers for each interface type:

Table 2-9 Switch Pack E39 (Z) Selections (Cont)

Switches	Function

Interface Type	SW5	SW6	SW7
RS-232-C, RS-423-A, Integral Modem*	OFF	OFF	OFF
V.35	ON	OFF	OFF
RS-422-A	OFF	OFF	ON

* Integral modem is selected by BC55A cable when installed in J1 of the M8203 line unit. Module connector J2 must not have a cable or test connector installed.

(Switches 8-10)

Line Speed Selection – Selects modem speed for Integral Modem applications, Null Modem applications, and diagnostic testing.

Switch				Switch			
Speed	8	9	10	Speed	8	9	10
1 MEG	ON	ON	ON	19.2K†	ON	ON	OFF
500K	OFF	ON	ON	9.6K	OFF	ON	OFF
250K	ON	OFF	ON	4.8K	ON	OFF	OFF
56K	OFF	OFF	ON	2.4K	OFF	OFF	OFF

† Normal switch setting unless the Integral Modem or Null Modem clock features are used.

Table 2-10 Switch Pack E121 (Y) Selections

Switches	Function
	NOTE **Switch OFF equals a logical one (1).**
1-8	Bootstrap Offset Address Selection – These switches are physically connected to IBUS Register 16 with switch 1 being the least significant bit (LSB) and switch 8 the most significant bit (MSB). When the remote load detect (RLD) feature is used, Switch Pack E121 (switches 1-8) must contain the appropriate offset entry address in the bootstrap program. The address formed by the DMR11 is 173XXX, where XXX is the content of E121, switches 1-8. Variations in bootstrap ROMs may require different entry addresses to boot the DMC11/DMR11. If the remote load detect, feature is not used, the offset must be set to octal 000, switches 1-8 all ON (closed). **NOTE** **When the RLD feature is used, the microdiagnostics in the bootstrap ROM must be disabled.**

Table 2-10 Switch Pack E121 (Y) Selections (Cont)

Switches	Function
	The following examples are for the M9301-YJ bootstrap module. Depending on the bootstrap module used, reference should be made to the appropriate manual for specific details. 1. *M9301-YJ Bootstrap Technical Manual* EK-M9301-TM-001 2. *M9312 Technical Manual*, EK-M9312-TM-002 To boot DMR11 unit 0 without CPU diagnostics, address 356 must be selected: Switch # (LSB … MSB): 1 2 3 4 5 6 7 8 / ON OFF OFF OFF ON OFF OFF OFF = 356 To boot DMR11 unit 1 without CPU diagnostics, address 374 must be selected: Switch # (LSB … MSB): 1 2 3 4 5 6 7 8 / ON ON OFF OFF OFF OFF OFF OFF = 374 To boot DMR11 unit 0 with CPU diagnostics, address 354 must be selected: Switch # (LSB … MSB): 1 2 3 4 5 6 7 8 / ON ON OFF OFF ON OFF OFF OFF = 354 To boot DMR11 unit 1 with CPU diagnostics, address 372 must be selected: Switch # (LSB … MSB): 1 2 3 4 5 6 7 8 / ON OFF ON OFF OFF OFF OFF OFF = 372
9	DMC Line Compatable – Switch is physically connected to IBUS Register 11, bit 2. The DMR11 microcode uses this bit to determine whether to implement DIGITAL Data Communications Message Protocol (DDCMP) version 4.0 or DMC Line Compatible Mode. • OFF = DMC11 Line Compatible Mode. • ON = DDCMP version 4.0, DMR11 Operating Mode.
10	High Speed Select – Switch is physically connected to IBUS Register 11, bit 1. **NOTE** **The combination of switches 9 and 10 must be appropriately selected to satisfy the configuration requirements as listed below.**

Table 2-10 Switch Pack E121 (Y) Selections (Cont)

Switches	Function

SW 9	SW 10	Configuration
ON	ON	DDCMP version 4.0 (not connected to DMC11) with line speed less than 1M b/s.
ON	OFF	DDCMP version 4.0 (not connected to DMC11) with line speed at 1M b/s.
OFF	ON	Connected to low speed DMC11-DA (M8200-YA)
OFF	OFF	Connected to high speed DMC11-AL (M8200-YB)

Table 2-11 Switch Pack E134 (X) Selections

Switches	Function

NOTE
Switch OFF equals a logical one (1).

1-8 Bootstrap Password Selection – These switches are physically connected to IBUS Register 15 with switch 1 being the least significant bit and switch 8 the most significant bit. In the DMR11, this switch will contain the bootstrap password if the bootstrap feature is being used. Otherwise, it will contain an octal 377 [switches 1 through 8 OFF (open)].

NOTE
A password of 377 will disable the RLD feature. Also, if the DMR11 is connected to a modem and the user program has not assigned Base In/Control In to the DMR11, when the DMR11 detects Ring Detect it will drop DTR to disable answering the call.

Example of a password of octal 012:

	LSB							MSB
Switches	1	2	3	4	5	6	7	8
	ON	OFF	ON	OFF	ON	ON	ON	ON

9 Auto-Answer Enable – When the switch is in the ON positon, auto-answer is disabled. The DMR11, following a power up or master clear, assests DTR allowing the DMR11 to answer an incoming call for remote load. The call terminates only when the user program issues a Halt Request or the remote end terminates the call.

When the switch is in the OFF position, auto-answer is enabled. This allows the DMR11 to monitor ring indicator (RI) and data set ready (DSR) to answer and control incoming calls. Control is established using a 20 second call set up timer. Refer to section 3.7.2.1 for additional information.

Table 2-11 Switch Pack E134 (X) Selections (Cont)

Switches	Function
	NOTE **If a DMR11 is installed on a switched line, this switch must be placed in the OFF position to allow the DMR11 to effectively control incoming calls.**
10	Microdiagnostic – Switch is physically connected to IBUS Register 11, bit 5. Microdiagnostic testing is executed when the conditions indicated below are met.

SEL 0 BIT 13*	SW10 AT E134 ON M8203	Execution of Microdiagnostics
Clear	ON	No Microdiagnostics Run
Clear	OFF	Run Microdiagnostics
Set	ON	Run Microdiagnostics
Set	OFF	NO Microdiagnostics Run

NOTE
When installing a DMR11 to run under DMC11 software, it is advisable to place this switch in the ON position. This is necessary where DMC11 software is not designed to wait 6.4 ms for microdiagnostic testing to be completed.

*At Master Clear time

2.6.1 M8203 Considerations

Configure all appropriate switch settings and jumpers on the M8203 line unit module according to the recommendations in Table 2-7.

NOTE
If the customer has additional requirements because of modem restrictions or a bootstrapping feature, be sure to configure the line unit to his requirements using the information contained in Tables 2-8 through 2-11.

Table 2-12 Cable Description

Interface	Description
RS-232-C	
• Cable Assembly: BC55C-10 (Refer to Figure 2-4A) • M8203 Connector: J2 • Test Connector: H325	A 3 m (10 feet) cable with a 40 pin, berg connector at one end which is installed into J2 of the M8203 so that the ribbed side of the cable faces out. This creates a half twist in the cable and is required for proper pin connections. The other end has a panel bracket that includes three different cinch connectors, J1, J2, and J3. Connector J2 is used for RS-232-C and is connected to the modem with external cable BC05D-25. The bracket must be mounted on the rear mounting rail of the cabinet to ensure proper grounding and for easy access to external cable connections. The BC55C panel contains several jumpers. Depending on the modem option selected, certain jumpers must be installed. Refer to Table 2-13 for detailed jumper configurations.
External Cable	
• BC05D-25 (Refer to Figure 2-4E) • Test Connector: H325	A 7.5 m (25 feet) external cable that connects J2 of the BC55C panel to an RS-232-C modem.
RS-422-A	
• Cable Assembly: BC55B-10 (Refer to Figure 2-4B) • M8203 Connector: J2 • Test Connector: H3251	A 3 m (10 feet) cable with a 40 pin, berg connector at one end which is installed into J2 of the M8203 so that the ribbed side of the cable faces out. This creates a half twist in the cable and is required for proper pin connections. This cable is similar to the BC55C in that it has a panel bracket at the other end. There is, however, only one connector on the panel (J2) that is used with cable BC55D-33 for external connection to the modem. The bracket must be mounted on the rear mounting rail of the cabinet to ensure proper grounding and easy access to external cable connections. The BC55B panel has two jumpers (W1 & W2) for shield grounding connections. Normally, W1 is always out (special application only) and W2 normally in. For RS-449 applications, W2 can be removed to place a 100 ohm resistor between circuit ground and frame ground to dissipate ground currents.
External Cable	
• BC55D-33 (Refer to Figure 2-4F) • Test Connector: H3251	A 10 m (33 feet) external cable that connects J2 of the BC55B panel to an RS-422-A modem.

Table 2-12 Cable Description (Cont)

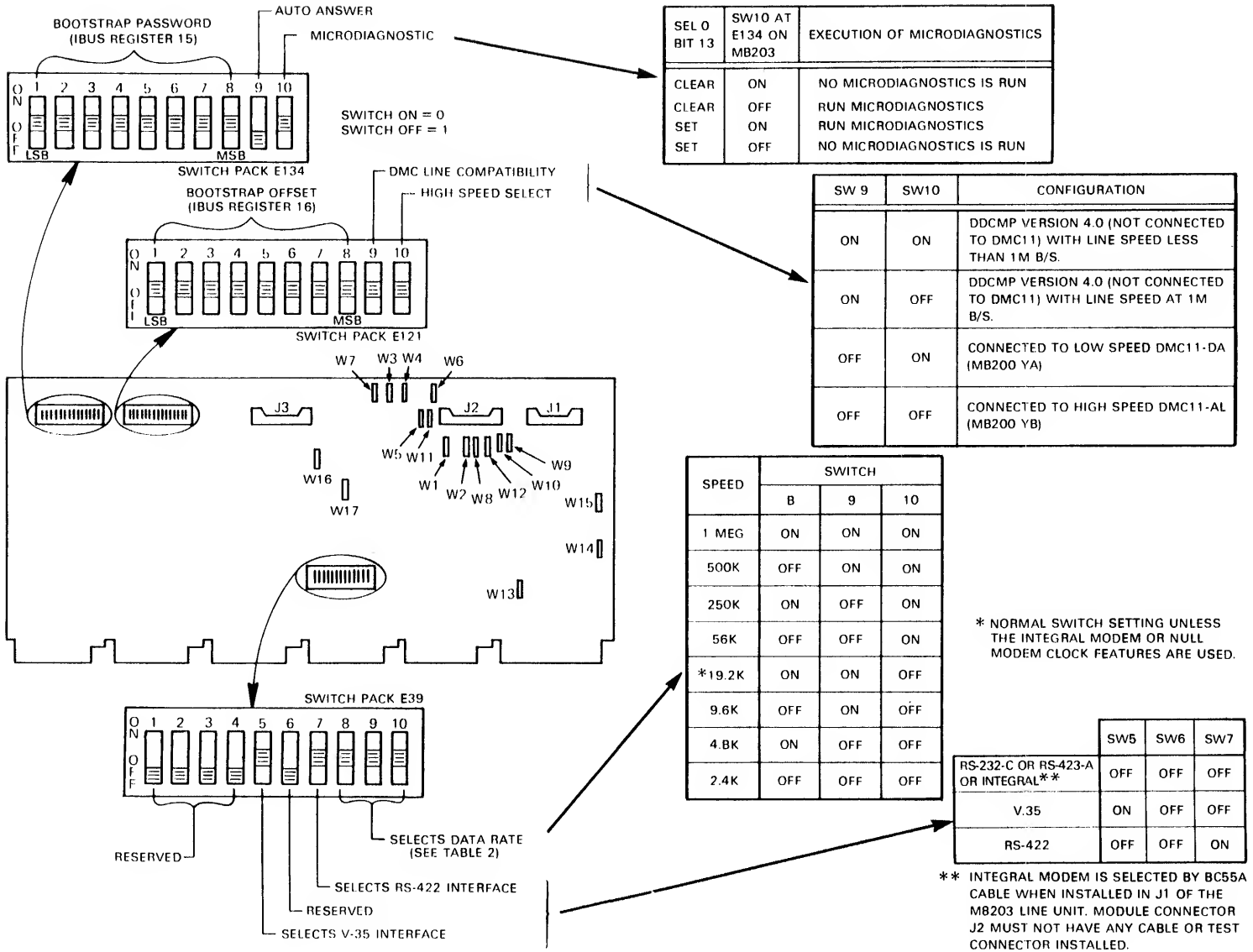
Interface	Description
RS-423-A • Cable Assembly: BC55C-10 (Refer to Figure 2-4A) • M8203 Connector: J2 • Test Connector: H3251	Same cable as used for RS-232-C except that panel connector J1 is used with external cable BC55D-33 for connection to the modem. The bracket must be mounted on the rear mounting rail of the cabinet to ensure proper grounding and easy access to external cable connections. The BC55C panel contains several jumpers. Depending on the modem option selected, certain jumpers must be installed. Refer to Table 2-13 for detailed jumper configurations.
External Cable BC55D-33 (Refer to Figure 2-4F) • Test Connector: H3251	A 10 m (33 feet) external cable that connects J1 of the BC55C panel to an RS-423-A modem.
V.35 • Cable Assembly: BC05Z-25 (Refer to Figure 2-4G • M8203 Connector: J1 • Test Connector: H3250	A 7.5 m (25 feet) modem cable with a 40 pin, berg connector at one end that connects to J1 of the M8203. A 37 pin, DataPhone Digital Service (DDS) connector is installed at the other end and connects to the modem.
Integral Modem • Cable Assembly: BC55A-10 (Refer to Figure 2-4C) • M8203 Connector: J1 • Test Connector: NONE (Place panel switch to HDX Position for turnaround)	A 3 m (10 feet) cable with a 40 pin, berg connector at one end that plugs into J1 of the M8203 with the cable strain relief tab facing out. A BC55A connector panel is installed at the other end. This panel contains four connectors, two female and two male. The panel also includes a toggle switch to select either full-duplex or half-duplex. The panel is mounted on the rear mounting rail of the cabinet to ensure easy access to external connections and for proper grounding. Appropriate terminator connectors H3257 or H3258 must be used. See Figures 2-7 and 2-8.

NOTE

Ensure that all cables mounted in the M8207 and M8203 are properly installed and seated in the berg connectors.

Table 2-12 Cable Description (Cont)

Interface	Description
External Cables	
• BC55N-98 (Refer to Figure 2-4D) • Test Connector: NONE	A 29.4 m (98 feet) external twinax cable used to interconnect a DMC11 to a DMR11 or a DMR11 to a DMR11 for a selected data rate of 56K b/s.
• BC55M-98 (Refer to Figure 2-4D) • Test Connector: NONE	A 29.4 m (98 feet) external triaxial cable used for the same purpose as the BC55N, but for data rates above 56K b/s.



SEL 0 BIT 13	SW10 AT E134 ON MB203	EXECUTION OF MICRODIAGNOSTICS
CLEAR	ON	NO MICRODIAGNOSTICS IS RUN
CLEAR	OFF	RUN MICRODIAGNOSTICS
SET	ON	RUN MICRODIAGNOSTICS
SET	OFF	NO MICRODIAGNOSTICS IS RUN

SW 9	SW10	CONFIGURATION
ON	ON	DDCMP VERSION 4.0 (NOT CONNECTED TO DMC11) WITH LINE SPEED LESS THAN 1M B/S.
ON	OFF	DDCMP VERSION 4.0 (NOT CONNECTED TO DMC11) WITH LINE SPEED AT 1M B/S.
OFF	ON	CONNECTED TO LOW SPEED DMC11-DA (MB200 YA)
OFF	OFF	CONNECTED TO HIGH SPEED DMC11-AL (MB200 YB)

SPEED	SWITCH		
	B	9	10
1 MEG	ON	ON	ON
500K	OFF	ON	ON
250K	ON	OFF	ON
56K	OFF	OFF	ON
*19.2K	ON	ON	OFF
9.6K	OFF	ON	OFF
4.8K	ON	OFF	OFF
2.4K	OFF	OFF	OFF

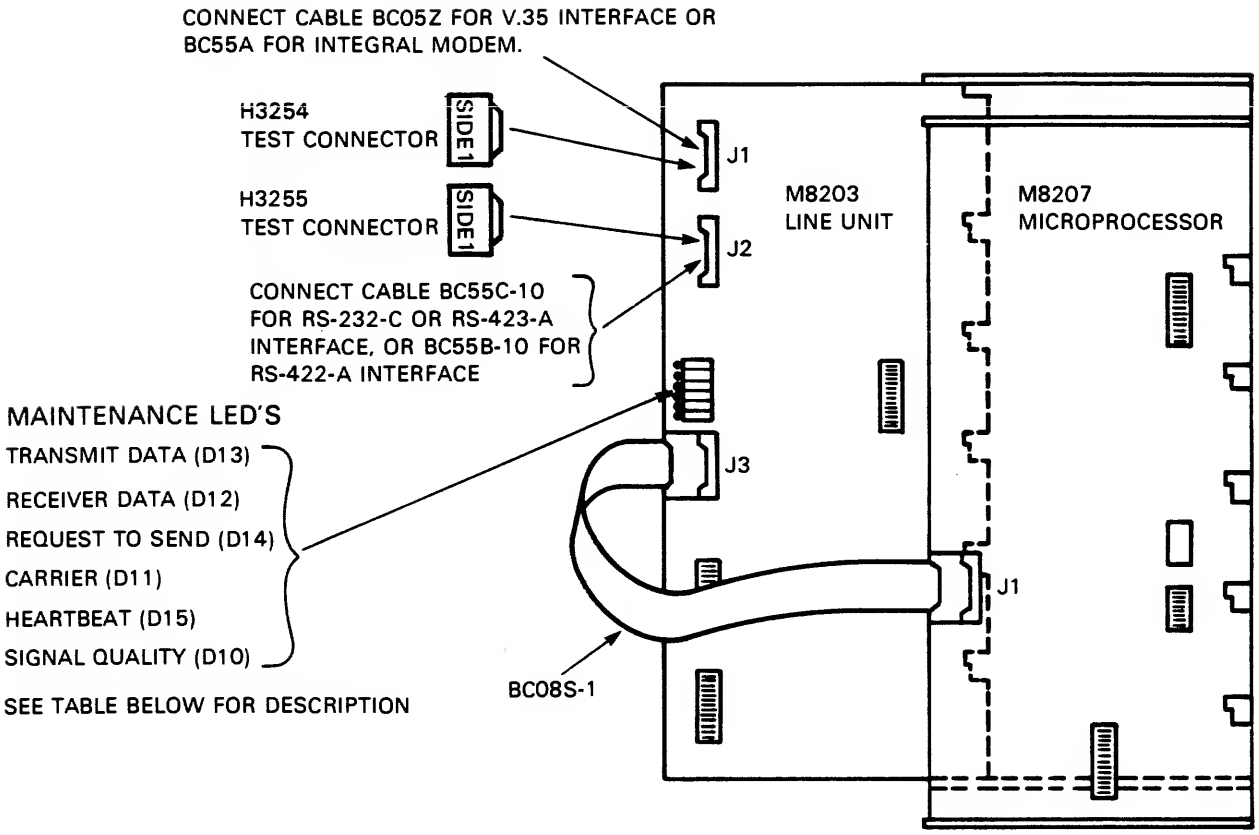
* NORMAL SWITCH SETTING UNLESS THE INTEGRAL MODEM OR NULL MODEM CLOCK FEATURES ARE USED.

	SW5	SW6	SW7
RS-232-C OR RS-423-A OR INTEGRAL**	OFF	OFF	OFF
V.35	ON	OFF	OFF
RS-422	OFF	OFF	ON

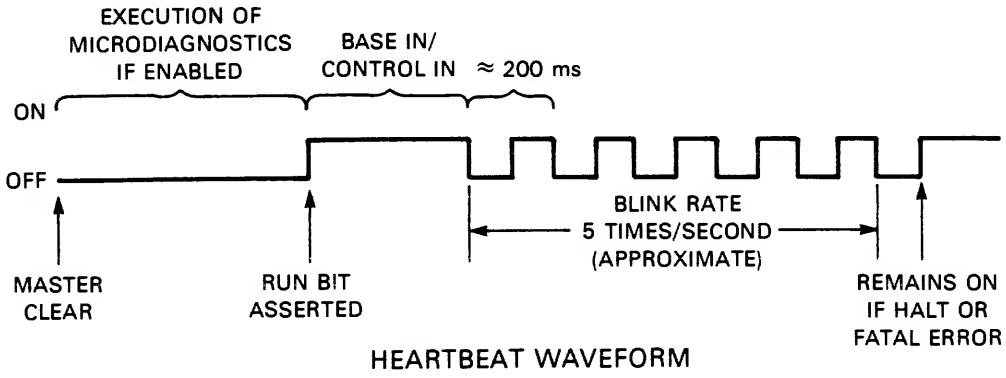
** INTEGRAL MODEM IS SELECTED BY BC55A CABLE WHEN INSTALLED IN J1 OF THE M8203 LINE UNIT. MODULE CONNECTOR J2 MUST NOT HAVE ANY CABLE OR TEST CONNECTOR INSTALLED.

MK 2119

Figure 2-2 M8203 Switch/Jumper Locations



DESIGNATION	DESCRIPTION
D13	ON INDICATES DMR11 IS TRANSMITTING A STEADY STREAM OF 1's.
D12	ON INDICATES DMR11 IS RECEIVING A STEADY STREAM OF 1's.
D14	ON INDICATES THE USYRT IS READY TO TRANSMIT WHEN CTS IS DETECTED.
D11	ON INDICATES CARRIER IS PRESENT AT THE RECEIVER.
D15	THE HEARTBEAT SEQUENCE IS GRAPHICALLY SHOWN IN THE WAVEFORM BELOW.
D10	ON INDICATES CARRIER PRESENCE AND OFF INDICATES CARRIER ABSENCE.



MK-1570

Figure 2-3 Microprocessor/Line Unit Installation

2.6.2 M8203 Insertion

With system power OFF, carefully insert the M8203 line unit module into the proper backplane slot (usually adjacent to the microprocessor) and perform the following:

1. Interconnect the line unit and the microprocessor using the BC08S-1 cable. One end of the cable is connected to J1 of the M8207-RA microprocessor module and the other end to J3 of the M8203 line unit module. Carefully fold the cable back to the right, tightly against the component side of either the microprocessor or line unit module, so as to fit it into the mounting box. Refer to Figure 2-3 for connector layouts.

2. Insert the appropriate module test connector into the correct line unit connector as specified in Table 2-7. Be sure to insert with "SIDE 1" (etched on the test connector) visible from the component side of the line unit. See Figure 2-3 for test connector orientation.

   Schematics and outline drawings of each test connector used with the DMR11 are provided in Figure 2-5.

3. Turn System power ON and perform voltage checks on the line unit backplane slot. Ensure that the voltages are within the specified tolerances as listed in Table 2-2.

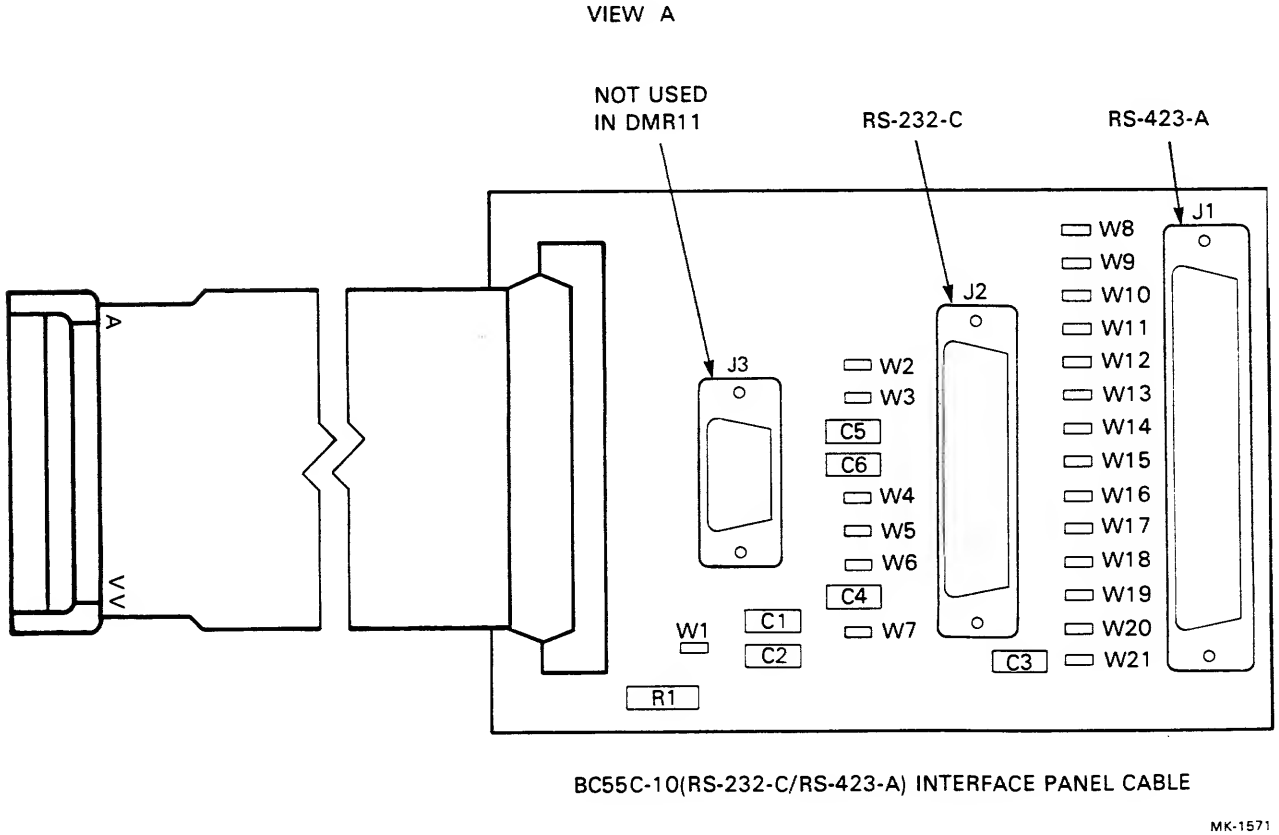
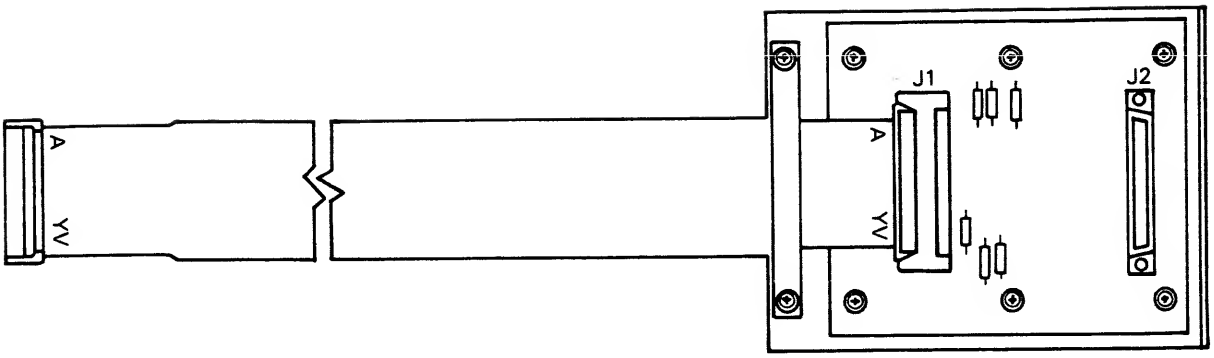


Figure 2-4 DMR11 Cable Drawings (Sheet 1 of 4)

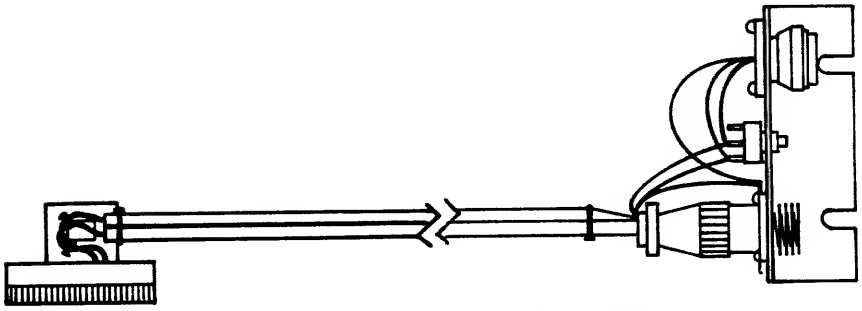
VIEW B



BC55B-10 (RS-422-A INTERFACE) PANEL CABLE

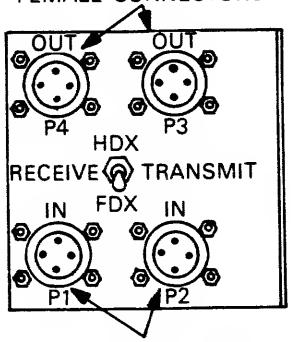
MK-2136

VIEW C



BC55A-10 (INTEGRAL MODEM) PANEL CABLE

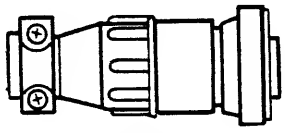
FEMALE CONNECTORS



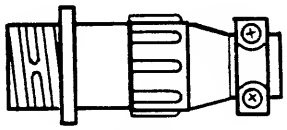
MALE CONNECTORS

CONNECTOR PANEL
(FRONT VIEW)

MK-2137



H3257
TERMINATOR



H3258
TERMINATOR

MK-2244

Figure 2-4 DMR11 Cable Drawings (Sheet 2 of 4)

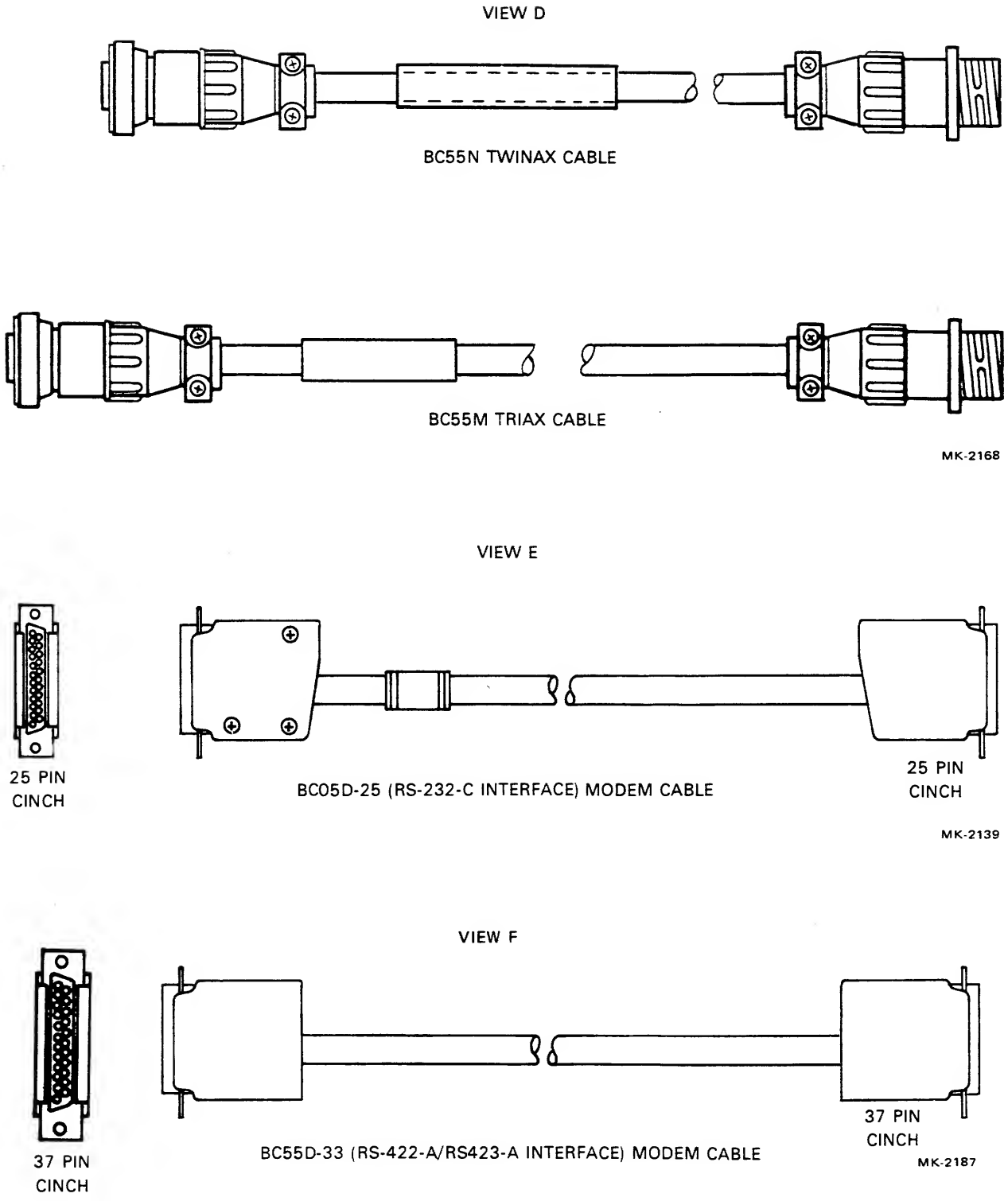


Figure 2-4 DMR11 Cable Drawings (Sheet 3 of 4)

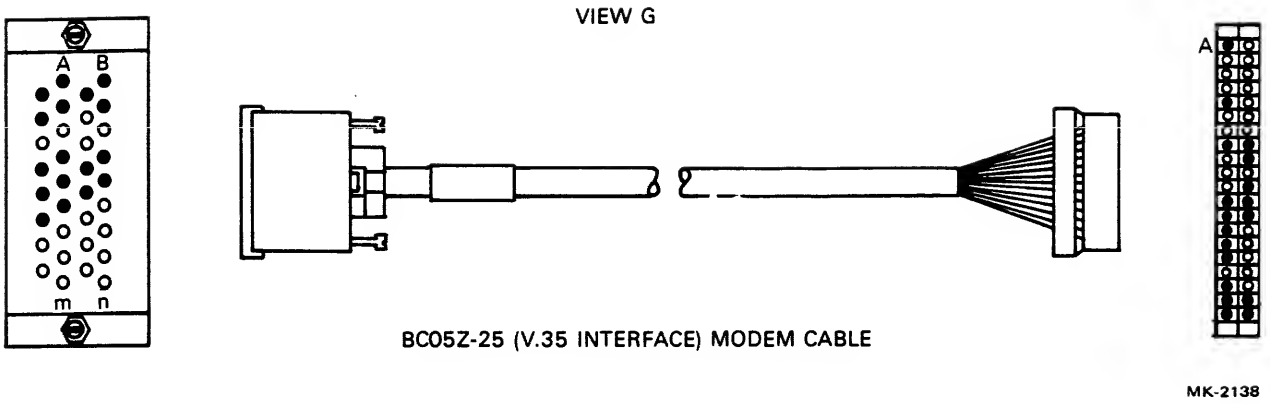


Figure 2-4 DMR11 Cable Drawings (Sheet 4 of 4)

4. Load and execute the M8203 static diagnostics, parts one and two, with external maintenance mode selected.

   A. PDP-11 System

      CZDMR* M8203 Static Diagnostic 1
      CZDMS* M8203 Static Diagnostic 2

   B. VAX-11/780 Systems

      EVDMA M8203 Repair Level Diagnostics
      REV *.*

   Chapter 4 provides detailed information on these diagnostic routines. Upon obtaining a minimum of five error free end passes, with the module turnaround test connector installed, proceed with step 5.

5. Remove the module turnaround test connector and connect the appropriate cable (see Table 2-7) to the proper berg connector for the DMR11 option selected. Refer to Table 2-12 for detailed information on cable requirements and to Figures 2-6 through 2-8 for system cabling configurations.

   NOTE

   When installing panel cables BC55A, BC55B, or BC55C, it is important that the panel be properly mounted to the rear mounting rail of the cabinet to ensure adequate grounding.

   When connecting the BC55C connector panel, verify that the appropriate modem jumpers on the panel are properly configured for the option selected. Table 2-13 lists each of these options and required jumper configurations.

   Integral Modem options require that a 75 ohm terminator be connected to each receive line (BC55A panel) at each end of a full-duplex and a half-duplex network. These terminators are available in both male (H3257) and female (H3258) types to accommodate different Integral Modem cabling. Selection of the appropriate terminator type is dependent upon which type of unused panel connector is available on the receive line at the BC55A-10 panel. Refer to Figure 2-7 for DMR11 to DMC11 cabling and to Figure 2-8 for DMR11 to DMR11 cabling.

Table 2-13 Modem Option Jumper Functions

J2 Pin	Jumper	RS-232C	Bell 208B	Bell 209	Data 2400	Datel 4800	CCITT V.23	CCITT V.26 BIS	CCITT V.27 TER	ISO 2110-1972 Future D		EIA RS-232	EIA RS-449	CCITT V.24
1	W1	IN	IN	IN	IN	IN				IN		AA		101
	W7													
2												BA	SD	103
3												BB	RD	104
4	W19	IN	IN	IN	IN	IN	IN	IN	IN	IN		CA	RS	105
5												CB	CS	106
6												CC	DM	107
7												AB	SG	102
8												CF	RR	109
9														
10														
11	W14									IN†			SF	126
12	W3	IN			IN	IN	IN	IN	IN	IN		SCF	SRR	122
13	W2	IN			IN		IN	IN	IN	IN		SCB	SCS	121
14	W6	IN			IN	IN	IN	IN	IN	IN		SBA	SSD	110
15	W20	IN	IN	IN	IN	IN	IN	IN	IN	IN		DB	ST	114
16	W5	IN			IN	IN	IN	IN	IN	IN		SBB	SRD	119
17	W18	IN	IN	IN	IN	IN	IN	IN	IN	IN		DD	RT	115
18	W17												LL	141
19	W4	IN			IN	IN	IN	IN	IN	IN		SCA	SRS	120
20												CD	TR	108
21	W16	IN		IN								CG	SQ	110
	W13												RL	140
22												CE	IC	125
23	W21	IN*			IN	IN	IN	IN	IN	IN		CH	SR	111
	W12	*										CI	SF	112
24	W15				IN								SS	116
	W10	IN	IN	IN		IN		IN	IN			DA	TT	113
25	W11				IN								SB	117
	W9												TM	142
	W8											Make Busy		

*RS-232-C defines both signals for this pin
† CCITT modem A only

6. Insert the appropriate cable turnaround test connector in the end of the cable. Refer to Table 2-7 for the specific test connector. Load and execute the M8203 static diagnostics specified in step 4 using the external maintenance mode selected to verify the module and cable. Upon obtaining a minimum of five error free passes, proceed to the DMR11 System Test Procedures, Section 2.7. Figure 2-5 illustrates the various test connectors used in the DMR11.

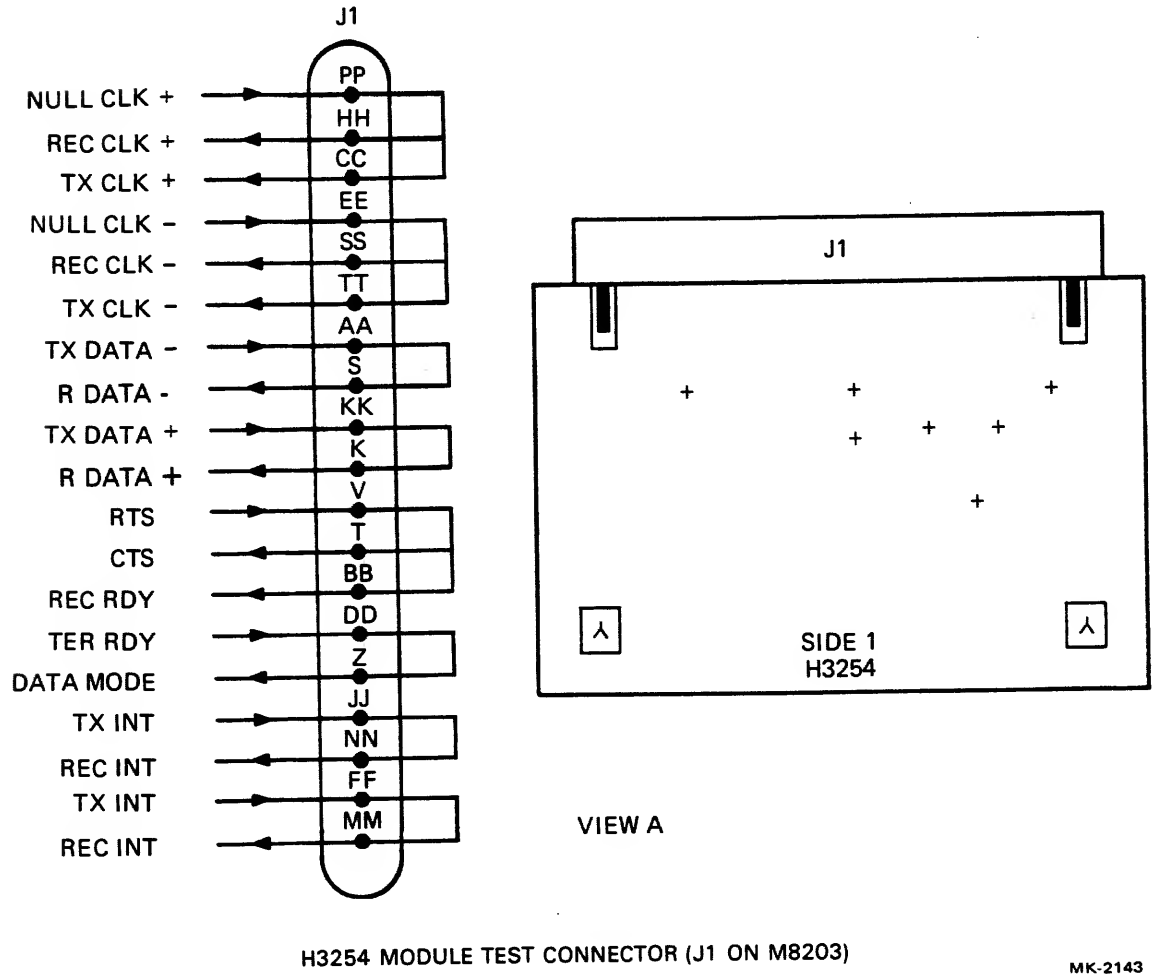


Figure 2-5 DMR11 Turnaround Test Connectors (Sheet 1 of 5)

2.7 DMR11 SYSTEM TESTING

The final step in the installation of a DMR11 subsystem is to exercise the microprocessor and line unit, as one complete unit, on the UNIBUS and over the communications link. This is the first testing that will use the DMR11 microcode.

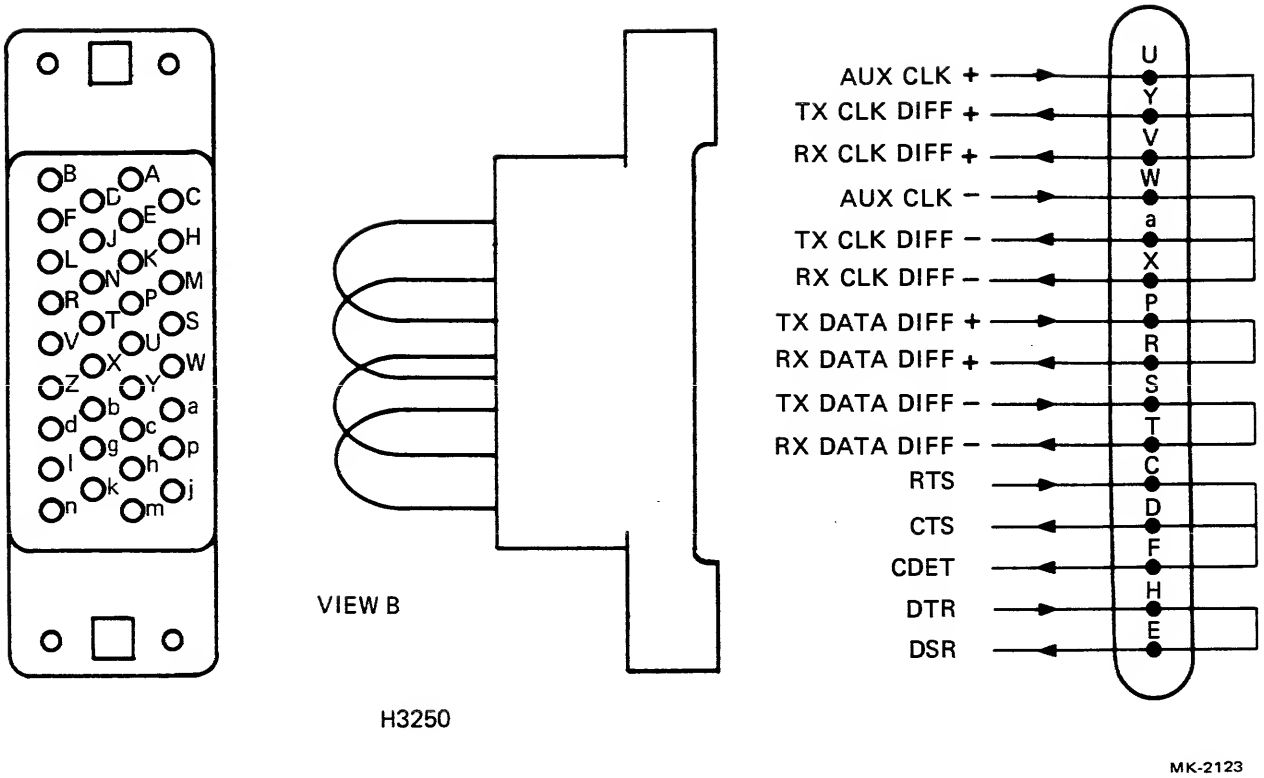


Figure 2-5 DMR11 Turnaround Test Connectors (Sheet 2 of 5)

2.7.1 Functional Diagnostic Testing

Ensure that the specific cable turnaround test connector for the selected DMR11 option is still installed at the end of the cable. Load and execute the DMR11 functional diagnostics with the External Mode selected. See Chapter 4 for details on this diagnostic test.

A. PDP-11 Systems

CZDMI* DMR11 Functional Diagnostics

B. VAX-11/780 Systems

EVDCA
REV *.* - VAX Synchronous Link Level 2 Diagnostics

Upon obtaining a minimum of five error free end passes, proceed to section 2.7.2.

2.7.2 DECX11 System Exerciser

The DECX11 system exerciser for the DMR11 can be run in two different operating modes, Internal and External. The External Mode selects faster UNIBUS activity. This mode also requires that the specific modem test connector is installed at the end of the cable and is the preferred mode of operation. Refer to Chapter 4 for additional details.

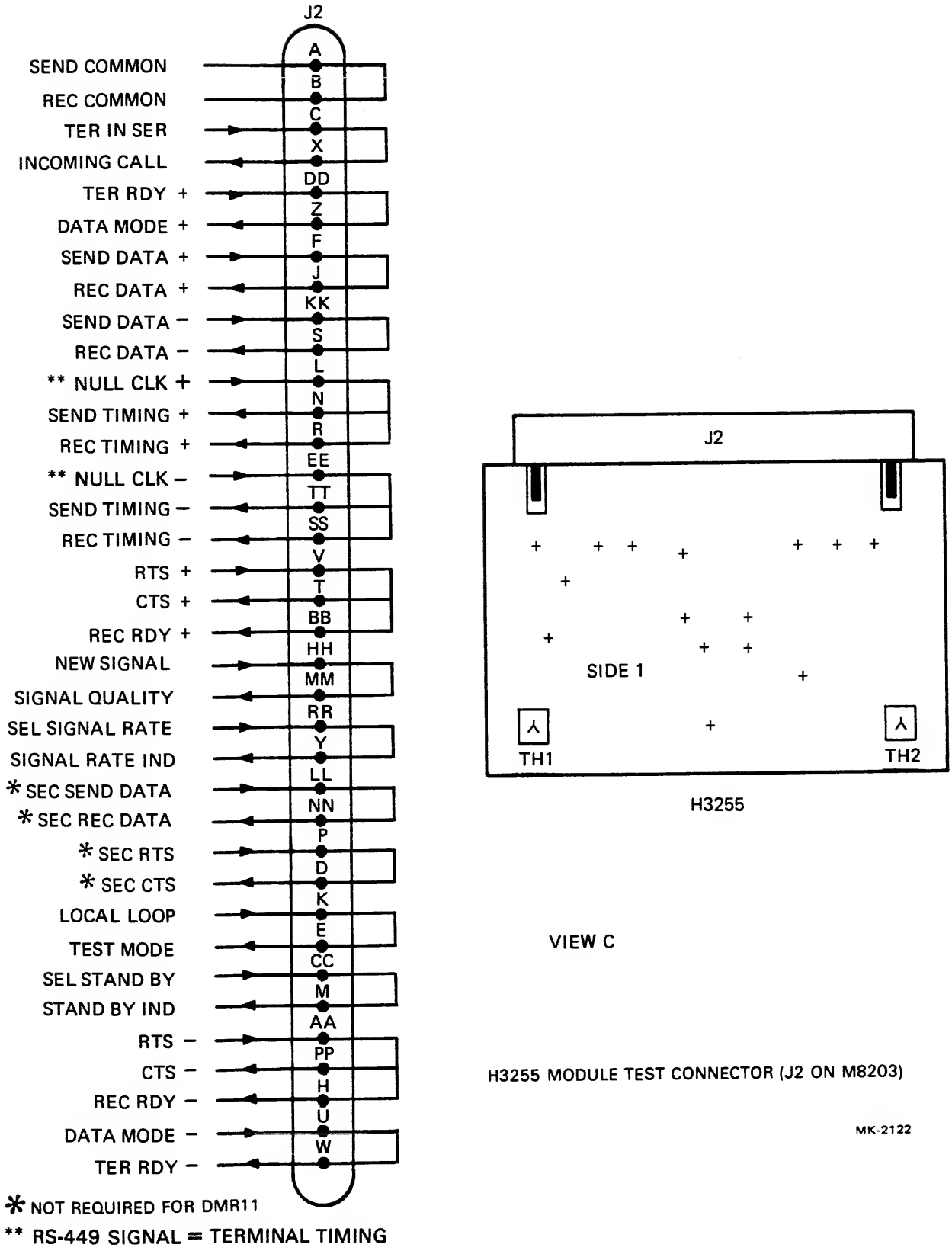


Figure 2-5 DMR11 Turnaround Test Connectors (Sheet 3 of 5)

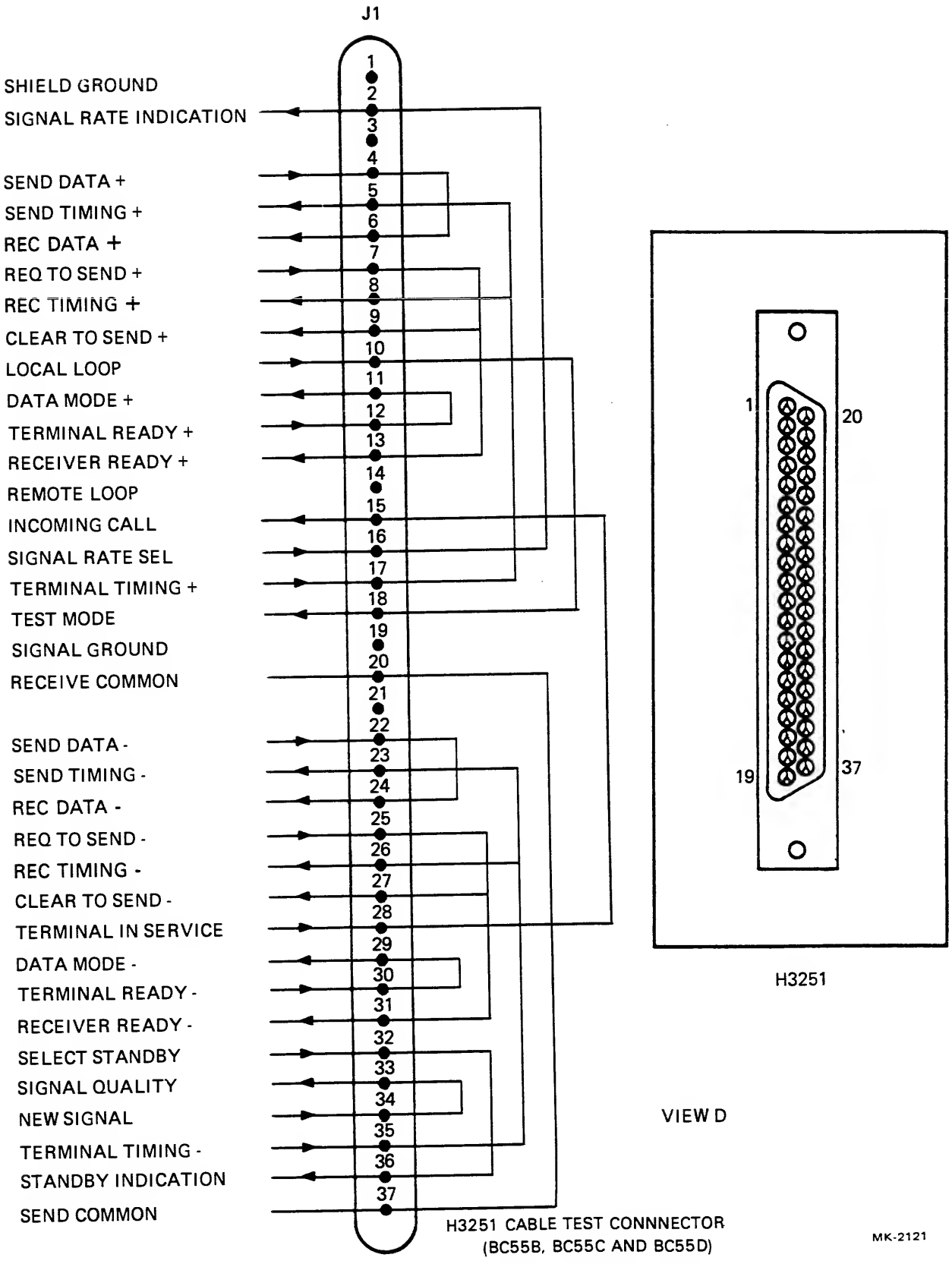


Figure 2-5 DMR11 Turnaround Test Connectors (Sheet 4 of 5)

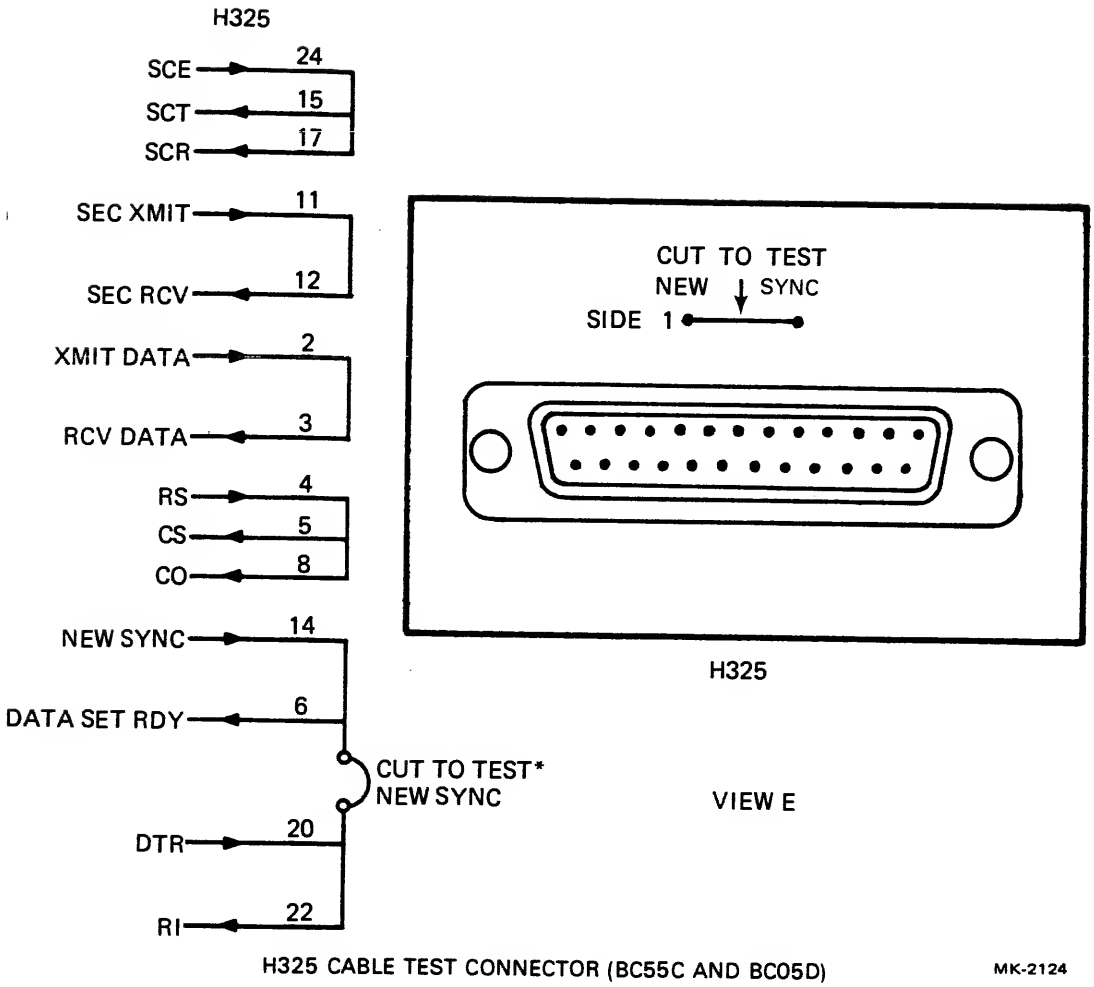


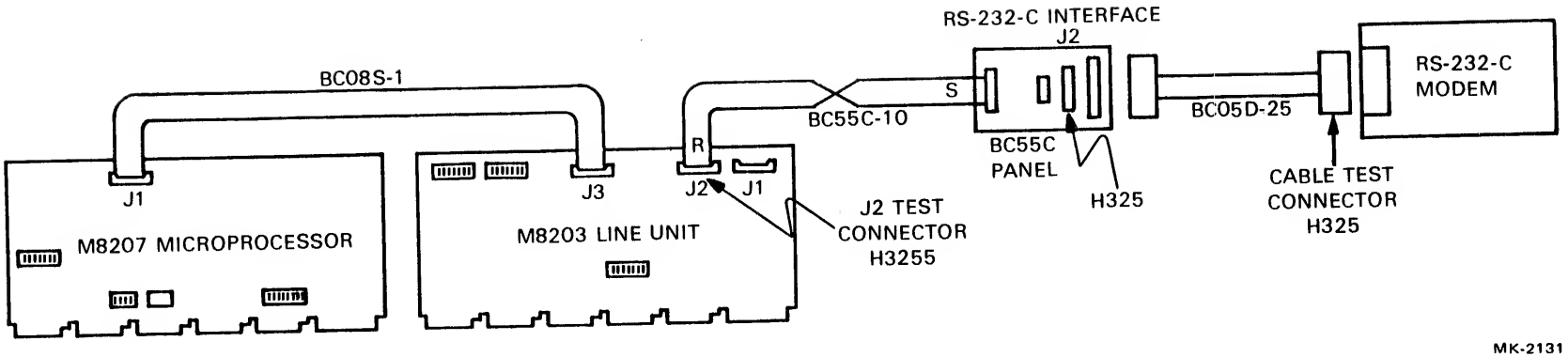
Figure 2-5 DMR11 Turnaround Test Connectors (Sheet 5 of 5)

2.7.3 Final Cable Connections

The final step in the installation process is to return the DMR11 to its normal cable connections, either to the appropriate modem or to the distribution panel. The DMR11 system cabling diagrams in Figures 2-6, 2-7, and 2-8, have been included to help show overall cabling for the various DMR11-XX options. References to specified locations of the various test connectors during diagnostic testing are also included. After the cables are connected to the appropriate modem or distribution panel, it is suggested that the Link Test Program ITEP be exercised.

2.7.4 DMR11 Link Testing

The DMR11 can be exercised over a communications link by the Interprocessor Test Program (ITEP). It is suggested that ITEP be configured to run first on a cable test connector and then on a modem with the modem Analog Loopback test feature selected, if the modem includes this feature. Next, the overall communications link should be exercised with the remote computer system that contains a DMR11 or a DMC11.



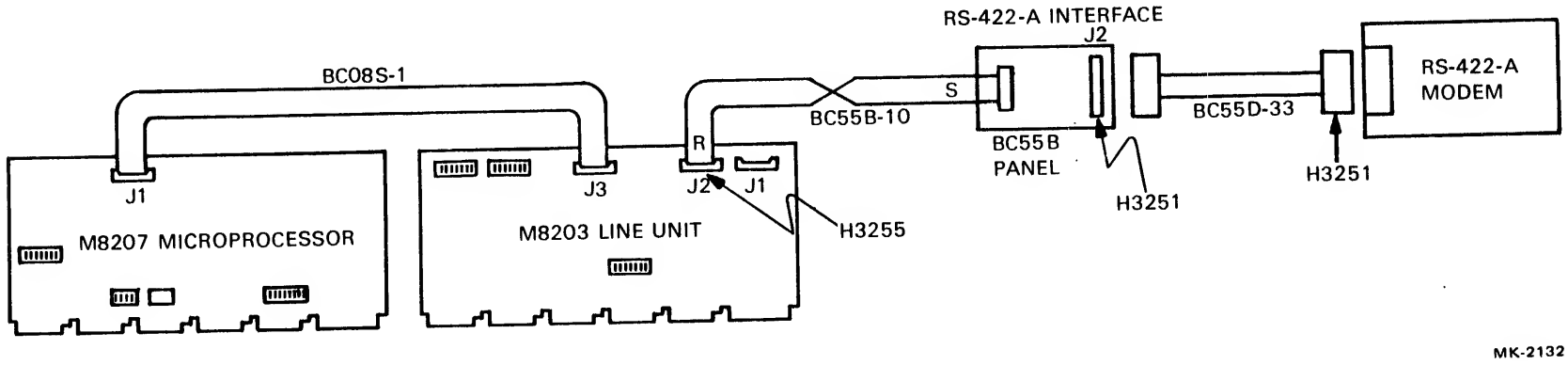


Figure 2-6 DMR11 Remote System Cabling Diagram (Sheet 1 of 2)

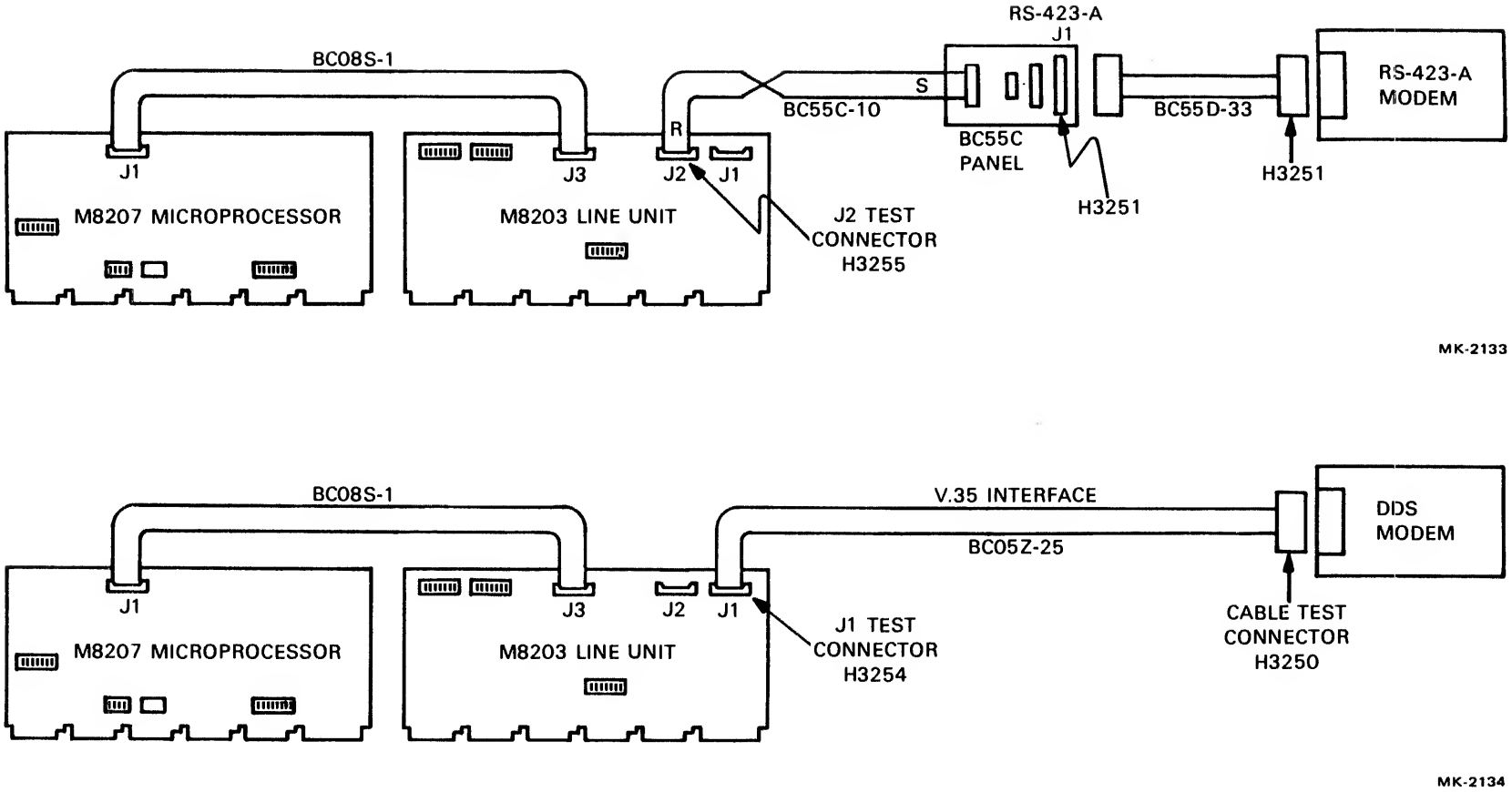


Figure 2-8 DMR-11 REMOTE SYSTEM CABLING

Figure 2-6 DMR11 Remote System Cabling Diagram (Sheet 2 of 2)

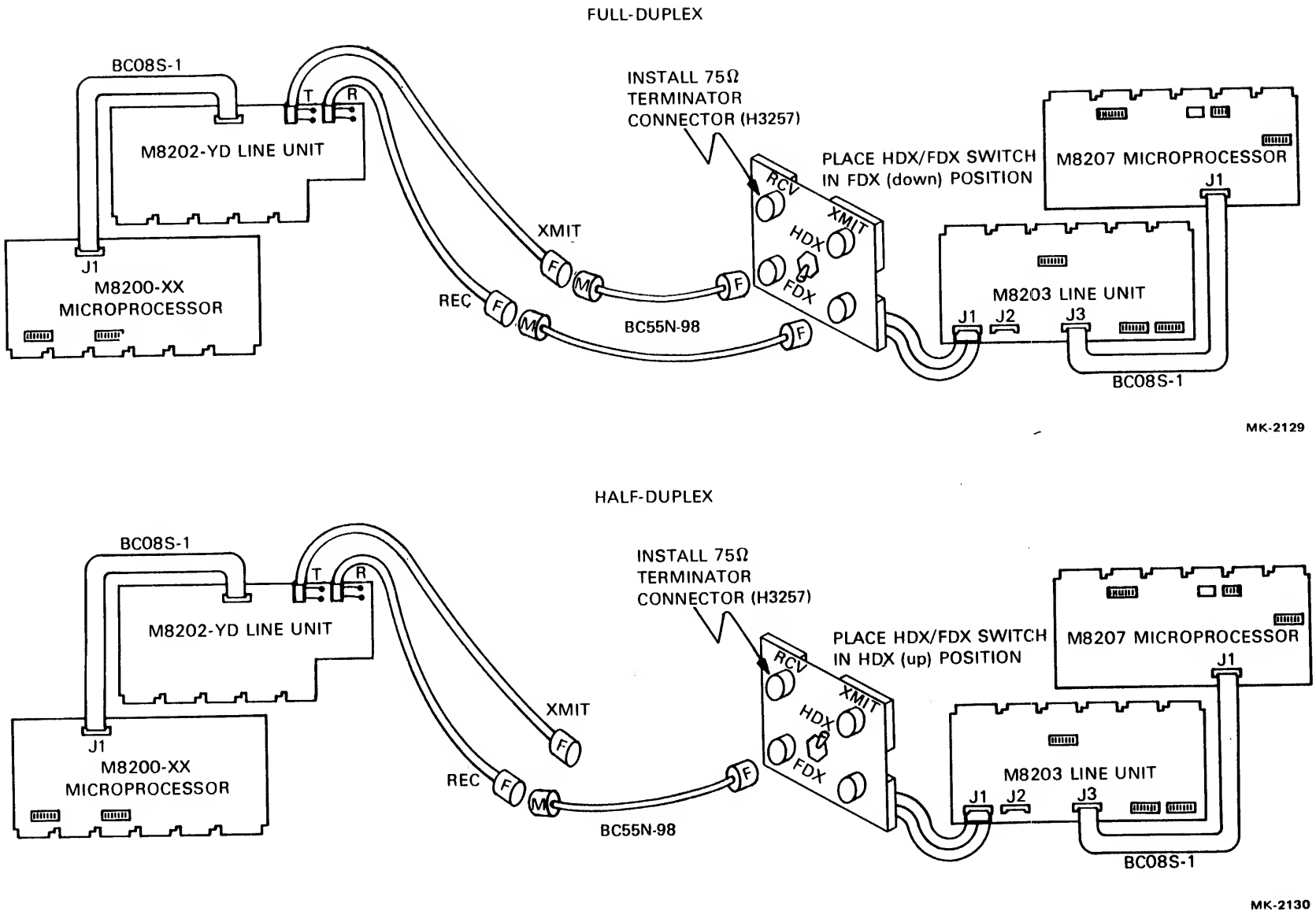


Figure 2-7 DMC11 to DMR11 Integral (Local) Modem Cabling Diagram

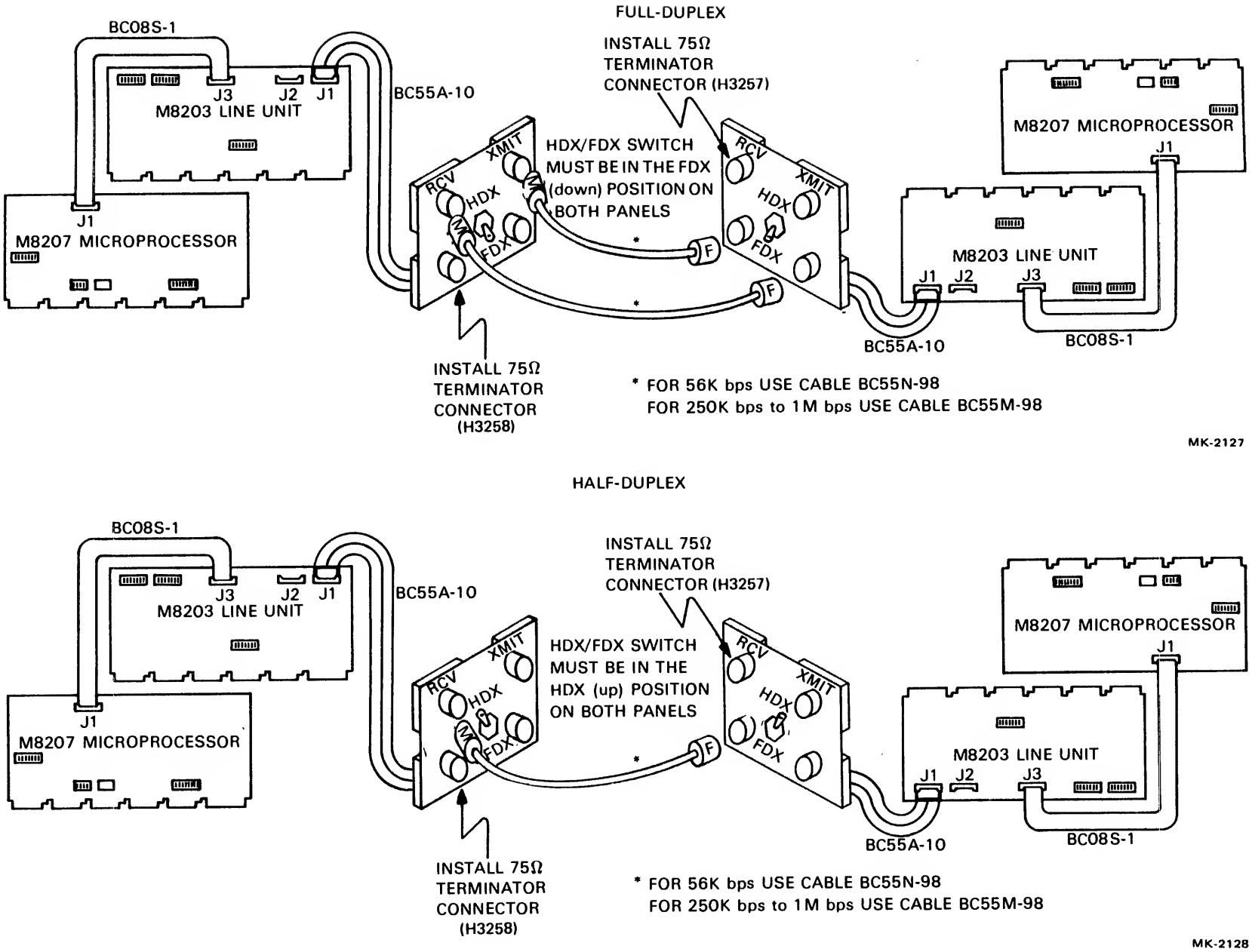


Figure 2-8 DMR11 to DMR11 Integral (Local) Modem Cabling Diagram

2.8 DMR11-XX INSTALLATION CHECK-OFF LIST

Date Completed

PHASE I – Preinstallation Considerations:

1. System placement (2.4.1.1) _____
2. Device placement (2.4.1.2) _____
3. System requirements (2.4.2)
   a. UNIBUS loading
   b. Power requirements
   c. Interrupt priority level
   d. DMR11 device address determination
   e. DMR11 vector address determination _____

PHASE II – Microprocessor Installation

1. Unpack DMR11 option and verify that all components were shipped (2.2 and Table 2-1). _____
2. With power ON, verify selected SPC backplane voltages (2.5.1 and Table 2-2). _____
3. Turn power OFF and remove NPR Grant (NPG) wire on selected SPC backplane slot (2.5.1). _____
4. Perform resistance checks to ensure that there are no shorts to ground on the backplane (2.5.1 and Table 2-2). _____
5. Ensure that the module is an M8207-RA and that W1 and W2 are correctly installed (2.5.2 and Table 2-3). _____
6. Install correct device address as determined in Phase I (2.5.2 and Table 2-4). _____
7. Install correct vector address as determined in Phase I (2.5.2 and Table 2.5). _____
8. Install correct switch selectable features (2.5.2 and Table 2-6). _____
9. Ensure that Priority Plug E77 is a BR5 and that it is properly installed (2.5.2). _____

Date Completed

10. Install microprocessor module M8207-RA into selected SPC slot (2.5.3). _____

11. Perform resistance checks on backplane to ensure that no shorts to ground exist on the module. Turn power ON and verify voltages (2.5.3 and Table 2-2). _____

12. Load and execute M8207 Static Diagnostics (2.5.3 and Chapter 4). _____

PHASE III – Line Unit Installation

1. Install the correct jumpers and switch selections for the appropriate DMR11 option. Use Table 2-7 to initially set up line unit and if additional features are required, refer to Tables 2-8 through 2-11 (2.6.1, Figure 2-2, and Table 2-7). _____

   Also refer to:

Table 2-8	Jumper Functions
Table 2-9	Switch Pack E39 Functions
Table 2-10	Switch Pack E121 Functions
Table 2-11	Switch Pack E134 Functions

2. Important switch/jumper verifications:

   a. If DMR11 is used with a DMC11, make sure Switch Pack E121, switch 9 is OFF (Table 2-10). _____

   b. If DMR11 is operating at a speed of 1M b/s, make sure Switch Pack E121, switch 10 is OFF (Table 2-10). _____

   c. If microdiagnostics are desired on initialization of the device, ensure that Switch Pack E134, switch 10 is in the appropriate position (Table 2-11). _____

   d. If down-line load or remote load detect feature is used, install the appropriate boot offset address in Switch Pack E121, switches 1-8, and the system password in Switch Pack E134, switches 1-8, at the remote end (Table 2-10 and Table 2-11). _____

NOTE

M9301-YJ or M9312 bootstrap module must be installed at the remote end.

		Date Completed
3.	With power OFF, carefully install the M8203 line unit adjacent to the microprocessor with interconnecting cable BC08S-1 in J3. The other end is installed in J1 of the M8207-RA microprocessor (2.6.2 and Figure 2-3).	_____
4.	Correctly insert the proper module test connector in J1 and/or J2 of the M8203 line unit (2.6.2, Figure 2-3 and Figure 2-6).	_____
5.	Turn Power ON, perform voltage checks, and adjust if necessary (2.6.2 and Table 2-2).	_____
6.	Load and execute the M8203 static diagnostics selecting module test connectors H3254 or H3255 (2.6.2 and Chapter 4).	_____
7.	Remove module test connector(s) and install the appropriate option cable to either J1 or J2, as required. When installing cables BC55A, BC55B, or BC55C, it is necessary to mount the connector panel on the rear mounting rail of the cabinet. It is important that the panel be properly mounted to ensure adequate grounding. Insert the appropriate turnaround test connector at the end of the cable.	_____
8.	Load and execute the M8203 static diagnostics in External Mode to verify cable connections (2.6.2, Table 2-7 and 2-12, and Figure 2-4 and 2-5).	_____

NOTE

On Integral Modem options, ensure that the 75 ohm receive line terminators are installed on the BC55A-10 panel as shown in Figure 2-7 or Figure 2-8.

PHASE IV - DMR11 System Testing

1.	With cable turnaround test connectors still installed, load and execute the DMR11 functional diagnostic test (2.7.1 and Chapter 4).	_____

	Date Completed
2. Configure and execute the DECX11 system exerciser to include the DMR11 option (2.7.2 and Chapter 4).	_____
3. Using ITEP, perform DMR11 link testing on the following (if possible): a. Cable test connectors installed b. Modem Analog Loopback test c. Link testing over network (2.7.4).	_____
4. Remove all cable test connectors, if installed, and connect appropriate cables to the modem or distribution panels (2.7.3, Figures 2-6, 2-7, and 2-8).	_____

CHAPTER 3
PROGRAMMING

3.1 INTRODUCTION

The information in this chapter is essential when developing a user program that will properly interface to the DMR11.

The command structure and format of input and output commands, as well as data port descriptions, are described in detail. Some examples of instruction sequences are also provided to demonstrate a typical method of user program implementation. Other discussions include special programming techniques, user access to maintenance mode, and user interpretation of status/error reporting.

3.2 COMMAND STRUCTURE

The command set for the DMR11 is structured into two categories; input commands and output commands. Brief descriptions of Input/Output commands, including command codes and the handshaking requirements, are provided in this section.

Transfer of control and status information between the main central processing unit (CPU) resident user program and the DMR11 is accomplished through four 16-bit UNIBUS control and status registers (CSR). Input commands are issued to the DMR11 by the user program and output commands are issued to the user program by the DMR11.

3.2.1 Control and Status Registers

Four 16-bit CSRs are used to transfer control and status information. These registers are both byte and word addressable. The eight bytes are assigned addresses in the floating address space in the I/O page as follows:

76XXX0, 76XXX1, 76XXX2, 76XXX3, 76XXX4, 76XXX5, 76XXX6 and 76XXX7.

For discussion, these byte addresses are designated Byte Select 0 through 7 (BSEL 0 through BSEL 7).

The four word addresses are the even numbered locations and are designated Select 0, 2, 4, and 6 (SEL 0, SEL 2, SEL 4, and SEL 6). It is recommended that the CSR address be assigned to the floating address space. Refer to Appendix A if detailed information on floating address space is required.

Figure 3-1 provides an overview of the CSR register format. Detailed bit descriptions of SEL 0 and BSEL 2 are contained in Tables 3-1 and 3-2 respectively.

Table 3-1 SEL 0 Bit Functions

Bits	Name	Description
0-3	Input Command Codes	Bits 0-2 define the type of input command issued by the user program to the microprocessor (see Table 3-3). Bit 3 is reserved for future expansion of the input command set.
4	Reserved	
5	Request In (RQI)	Serves as an interlock bit when requesting the use of the data port – set by the user program to request the data port. It is cleared by the program when the data port has been loaded.
6	Interrupt Enable In (IEI)	When set, allows the DMR11 to interrupt to vector address XX0, when RDI (bit 7 of BSEL 0) is set.
7	Ready In (RDI)	RDI is a DMR11 response to RQI, indicating to the program that it may load the data ports (SEL 4, SEL 6). It is cleared by the DMR11 indicating that the data port has been read and the input command transfer is complete.
8	Step Microprocessor (Step μP)	When set, this bit steps the microprocessor through one instruction cycle. The Run flip-flop should be cleared before executing this control function.
9	ROM Input (ROM IN)	When set, directs the contents of SEL 6 as the next microinstruction to be executed by the microprocessor when Step μP or Run is asserted.
10	ROM Output (ROM OUT)	When set, modifies the source paths for SEL 6 to be the contents of the addressed control read only memory (CROM) or the next microinstruction executed when Step μP is asserted.
11	Line Unit (LU LOOP)	When asserted, connects the line unit serial line out back into the serial line in. This is done at the TTL level, before level conversion. When the Line Unit Loop bit is set and Run is cleared, the STEP LU clock is the only clock available for shifting data out or in. When LU Loop and Run are set, data is clocked at the maintenance clock rate (approximately 48K b/s).

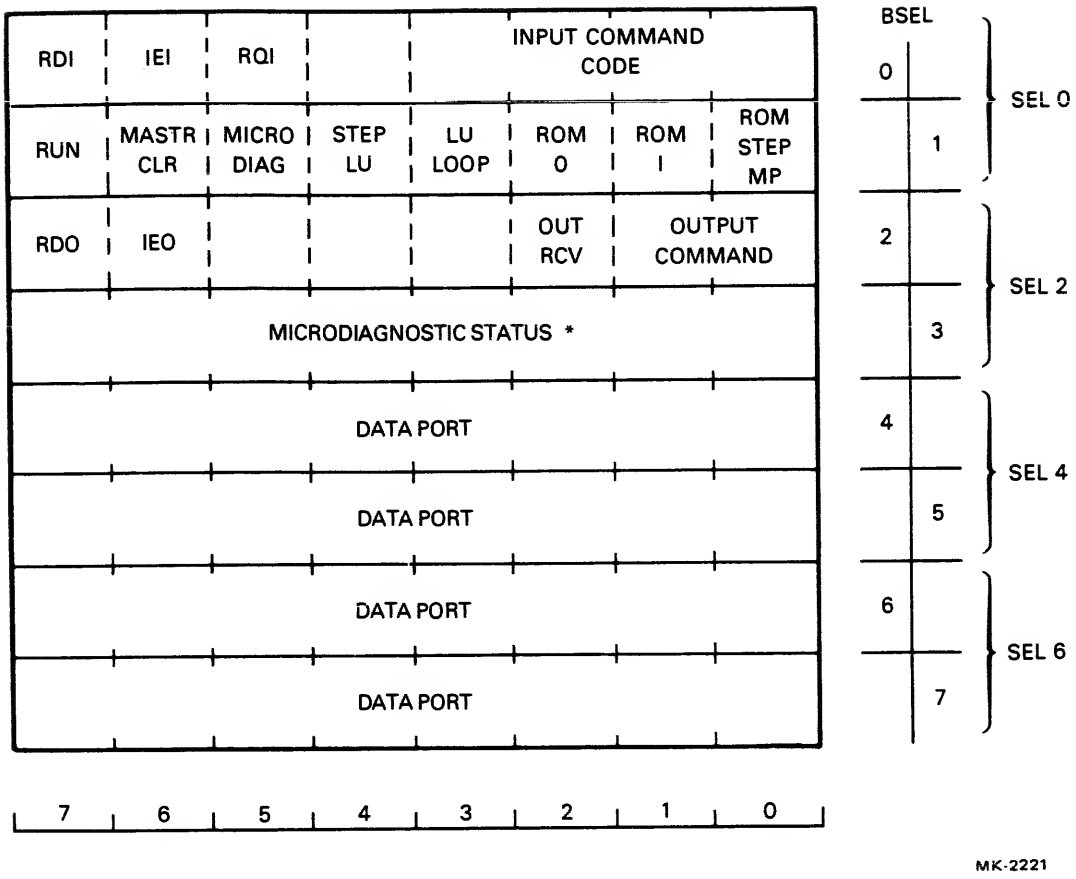
Table 3-1 SEL 0 Bit Functions (Cont)

Bits	Name	Description
12	Step Line Unit	Used in conjunction with LU Loop. When asserted, the transmitter shifts. When cleared, the receiver shifts.
13	Microdiagnostics (MICRO DIAG)	This bit controls automatic execution of internal microdiagnostics at Master Clear time. Depending on the position of switch 10 of Switch Pack E134 (M8203 line unit) either the Set or Cleared condition of this bit can enable this feature. Refer to the chart below for specific conditioning.

SEL 0 BIT 13*	SW 10 AT E134 ON M8203	Execution of Microdiagnostics
Clear	ON	No Microdiagnostics Run
Clear	OFF	Run Microdiagnostics
Set	ON	Run Microdiagnostics
Set	OFF	No Microdiagnostics Run

14	Master Clear	When set, Master Clear initializes both the microprocessor and the line unit. This bit is selfclearing. The microprocessor clock is enabled, and the Run flip-flop is asserted. The microprocessor's program counter is also temporarily cleared by Master Clear.
15	Run	On power up reset or device Master Clear, this bit is set by the DMR11 microcode to inform the user program that the DMR11 is ready to accept input commands. Run can be cleared for maintenance states.

*At Master Clear time.



*Valid only immediately after Master Clear or Reset.

Figure 3-1 UNIBUS Control and Status Registers Format Overview.

3.2.2 Initialization

Initialization places both the DMR11 hardware and firmware in the initialized (operational) state. In the initialized state, the DMR11 does not send or receive messages, but it does check for Enter MOP messages and for remote load detect (RLD).

Initialization is accomplished by one of the following methods:

1. System Initialization –
   - System Reset
   - Power-up/shut-down sequence
2. By the user program – Set Master Clear bit (BSEL 1)

Initialization of the DMR11 by the user program is done in two steps. The Master Clear bit is set, and then waits for the DMR11 to set the Run bit. Once the Run bit is set the DMR11 is ready to accept Base In.

Table 3-2 BSEL 2 Bit Functions

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>0, 1, 2</td><td>Output Command</td><td>These bits define the type of data transfer from the microprocessor to the user program:
<table>
<tr><th>Bit 2</th><th>Bit 1</th><th>Bit 0</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Transmit Buffer Address/ Character Count Out (TBA/CCO)</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Receive Buffer Address Character Count Out (RBA/CCO)</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Control Out</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Reserved</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>3-5</td><td>Reserved</td><td></td></tr>
<tr><td>6</td><td>Interrupt Enable Out (IEO)</td><td>When set, enables the DMR11, upon asserting RDO, to generate an interrupt to vector address XX4.</td></tr>
<tr><td>7</td><td>Ready Output (RDO)</td><td>Asserted by the DMR11 to indicate that the data ports (SEL 4 and SEL 6) contain data for the output command defined by bits 0-2 of BSEL 2. Bit 7 must be cleared by the user program after the data port is read.</td></tr>
</table>

Internal microdiagnostic testing is automatically executed at this time (during power-up/initialization) providing that this feature is appropriately enabled as described below:

SEL 0 BIT 13*	SW10 AT E134 ON M8203	Execution of Microdiagnostics
Clear	ON	No Microdiagnostics Run
Clear	OFF	Run Microdiagnostics
Set	ON	Run Microdiagnostics
Set	OFF	No Microdiagnostics Run

*At Master Clear time.

If microdiagnostic testing is disabled, the Run bit will be asserted by the DMR11 in about 240 microseconds. However, if enabled, the Run bit will be asserted (if tests pass) in about 6.4 milliseconds.

Test results (listed below) are available to the user program in BSEL 3. The program must check BSEL 3 before proceeding with Base In. If the tests fail, the DMR11 will not assert the Run bit and further operations are prohibited. Corrective action by authorized Field Service personnel is required. For additional information on microdiagnostic test, refer to section 4.5.4.

BSEL1	BSEL3	Indication
Run bit	200_8	Test Complete
Run bit	100_8	Test Inhibited
no Run bit	001_8 or XXX	M8207 Test Failed
no Run bit	002_8	M8203 Test Failed

Programming Example:

```
        MOV     #40000,SEL0     ;SET MASTER CLEAR
1$:     BIT     SEL0            ;TEST RUN BIT
        BPL     1$              ;BRANCH IF NOT READY YET
                                ;CHECK BSEL3 FOR MICRODIAGNOSTIC
                                ;STATUS
                                ;PROCEED WITH BASE IN
```

NOTE

If the Run bit is not asserted within 6.4 milliseconds, either the M8207 or the M8203 test may have failed and the user should check BSEL 3.

3.2.3 Input Commands Overview

In general, input commands provide the means for the user program operational modes to assign receive or transmit buffers to the DMR11. Detailed field descriptions and formats of each input command are provided in section 3.3.

Input commands are executed by the user program by requesting service and by setting the appropriate bits of the command code in bits 0-3 of BSEL 0. Specific handshake requirements to implement command transfers are explained in section 3.2.3.1.

Input commands are listed in Table 3-3. The Base In command is the only command that the program can issue, without causing a procedural error, following intialization.

Table 3-3 Input Commands

Input Commands	BSEL0			
	Bit 3	Bit 2	Bit 1	Bit 0
Transmit Buffer Address/ Character Count In	0	0	0	0
Control In	0	0	0	1
Halt	0	0	1	0
Base In	0	0	1	1
Receive Buffer Address/ Character Count In	0	1	0	0

The Base In command must be followed by Control In, then Receive Buffer Address/Character Count In (RBA/CCI), and then Transmit Buffer Address/Character Count In (TBA/CCI). Section 3.5, Programming Techniques, further defines proper command sequencing.

3.2.3.1 Input Command Handshaking

At start up time, before the user program can execute any input command, it must initialize the DMR11. This is accomplished by the program setting the Master Clear bit in BSEL 1 and waiting for the DMR11 to set the Run bit.

Input command sequencing requires that Base In be the only input command used following initialization. This command must be followed by Control In, Receive Buffer Address/Character Count In, and Transmit Buffer Address/Character Count In, respectively.

All input commands are issued by the user program in two successive steps. The first step requests the use of the data ports. The second step identifies the command type and the data port information for the appropriate command. The specific content of each data port is further defined under each command description in section 3.3. The handshaking procedure for input commands is as follows. (A typical programming example for an input command assignment is provided in Figure 3-2. The flow chart in Figure 3-3 further defines this process.)

The user program:

- Requests the use of the data port to issue an input command by setting Request In (RQI) bit 5 of BSEL 0. The user may also set bit 6 of BSEL 0, Interrupt Enable In (IEI), at the same time (using the same instruction) to allow the DMR11 to interrupt the CPU when the data port is available.

NOTE

1. **Because of interrupt and service time, it is most efficient for the user program to have input interrupts disabled and to simply scan RDI a few times (for less than 50 μs). If RDI is not set by the DMR11 in 50 μs, the user should set the IEI bit twice and wait for an interrupt.**

2. **When setting the IEI bit, the user program must use two consecutive bit set byte (BISB) instructions.**

3. **If interrupt mode is not used, the user must scan for Ready Out (bit 7 of BSEL 2) while waiting for RDI to set. The user program must be prepared to accept an output transfer from the DMR11 while it is waiting for RDI.**

- When the Data Port is available, the DMR11 informs the user by setting Ready In (bit 7 of BSEL 0) and, if IEI was previously set, the DMR11 generates an interrupt to vector XX0.
- If modem status is desired, the user can, at this time, read SEL 4 and SEL 6 for modem status.
- On detecting RDI bit set, the user can load the input command code into bit 0-3 of BSEL 0 and also load the appropriate information into SEL 4 and SEL 6.
- The user must then clear RQI (bit 5 of BSEL 0) to inform the DMR11 to decode the input command.
- When the DMR11 has read and decoded the input command, it clears RDI (BSEL 0, bit 7). This completes input command handshaking.

3.2.3.2 Modem Status Read – This feature provides the user program with the option of reading (monitoring) modem status during an input command. Modem status is updated by the DMR11 to SEL 4 and SEL 6 each time RDI is asserted in response to RQI.

Modem status is not guaranteed to be accurate prior to asserting RDI or after the program clears RQI. Sensing RDI set, the user program can read the status before loading the data port(s) for the particular command being executed.

Figure 3-4 shows the format for the modem status read feature. Table 3-4 lists the bit descriptions of modem status read for all four data ports.

```
INPUT COMMAND ASSIGNMENT ROUTINE:

THIS ROUTINE COULD BE ENTERED VIA THE FOLLOWING CONDITIONS:

        1. APPLICATION PROGRAM ISSUES AN INPUT COMMAND.
        2. AT THE COMPLETION OF THE INPUT COMMAND OR OUTPUT
           COMMAND PROCESSING BY THE DMR11 DRIVER, THERE ARE
           SOME OUTSTANDING INPUT COMMANDS WAITING TO BE ISSUED
           TO THE DMR11.


ASSUMPTIONS:
        - : R4 = CONTAINS DMR11 CSR ADDRESS (SEL 0).
        - : R5 = SCRATCH REGISTER.
        - : ICMD:       .WORD   ; ICMD10 -- INPUT COMMAND CODE
                        .WORD   ; ICMD12 -- INFORMATION FOR SEL4.
                        .WORD   ; ICMD14 -- INFORMATION FOR SEL6.

        - : MDMS:       .WORD   ; MODEM STATUS 1.
                        .WORD   ; MODEM STATUS 2.

        - : OUTPUT INTERRUPT IS ENABLED AT ALL TIMES.

INPUT:  BITB    # RQI,0(R4)        ; IS RQI ALREADY SET?
        DNE     EXIT              ; YES - PREVIOUS INPUT IS NOT DONE YET
                                  ;
        MOV     #4,R5             ; SET UP THE WAIT LOOP COUNT
10$:    BITB    #RDI,0(R4)        ; IS RDI CLEARED ?
        BEQ     20$               ; YES - CONTINUE WITH THE INPUT


        DEC     R5                ; SOME MORE WAITING ?
        BNE     10$               ; YES -
        BR      EXIT              ;
                                  ;
20$:    MOV     #4,R5             ; SET UP THE WAIT LOOP COUNT
        BISB    #RQI,0(R4)        ; NOW - SET THE RQI.
30$:    BITB    #RDI,0(R4)        ; IS RDI SET ?
        BNE     SETINP            ; YES - GO ISSUE THE INPUT NOW
        DEC     R5                ; SOME MORE WAITING ?
        BNE     30$               ; YES
                                  ; RDI WAIT LOOP EXPIRED
40$:    BISB    #IEI!RQI,0(R4)    ; SET INTERRUPT ENABLE
        BISB    #IEI!RQI,0(R4)    ; AGAIN
EXIT:   RETURN                    ;

        CAN ALSO BE ENTERED FROM AN INPUT INTERRUPT ROUTINE AFTER
        VERIFYING THAT RQI AND RDI ARE BOTH SET.

SETINP: MOV     4(R4), MDMS+0     ; GET MODEM, STATUS NOW
        MOV     6(R4), MDMS+2     ;
        BISB    ICMD+0,0(R4)      ; SET THE INPUT COMMAND CODE
        MOV     ICMD+2,4(R4)      ; LOAD DATA PORT SEL4
        MOV     ICMD+4,6(R4)      ; LOAD DATA PORT SEL6
        BICB    # RQI!IEI 0(R4)   ; CLEAR RQI AND IEI
        RETURN
                                                          MK-2245
```

Figure 3-2 Programming Example for Input Commands

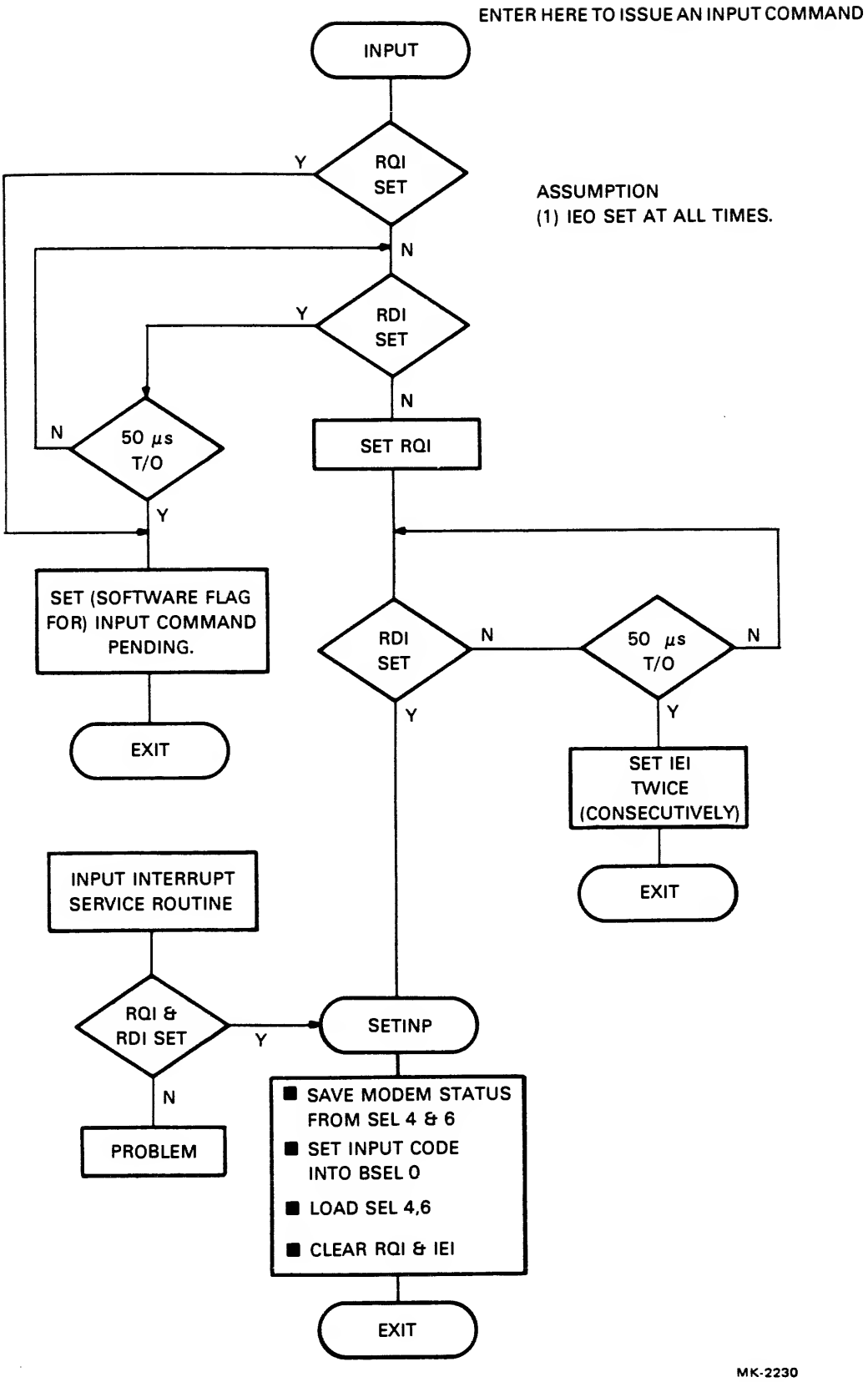


Figure 3-3 Input Command Servicing

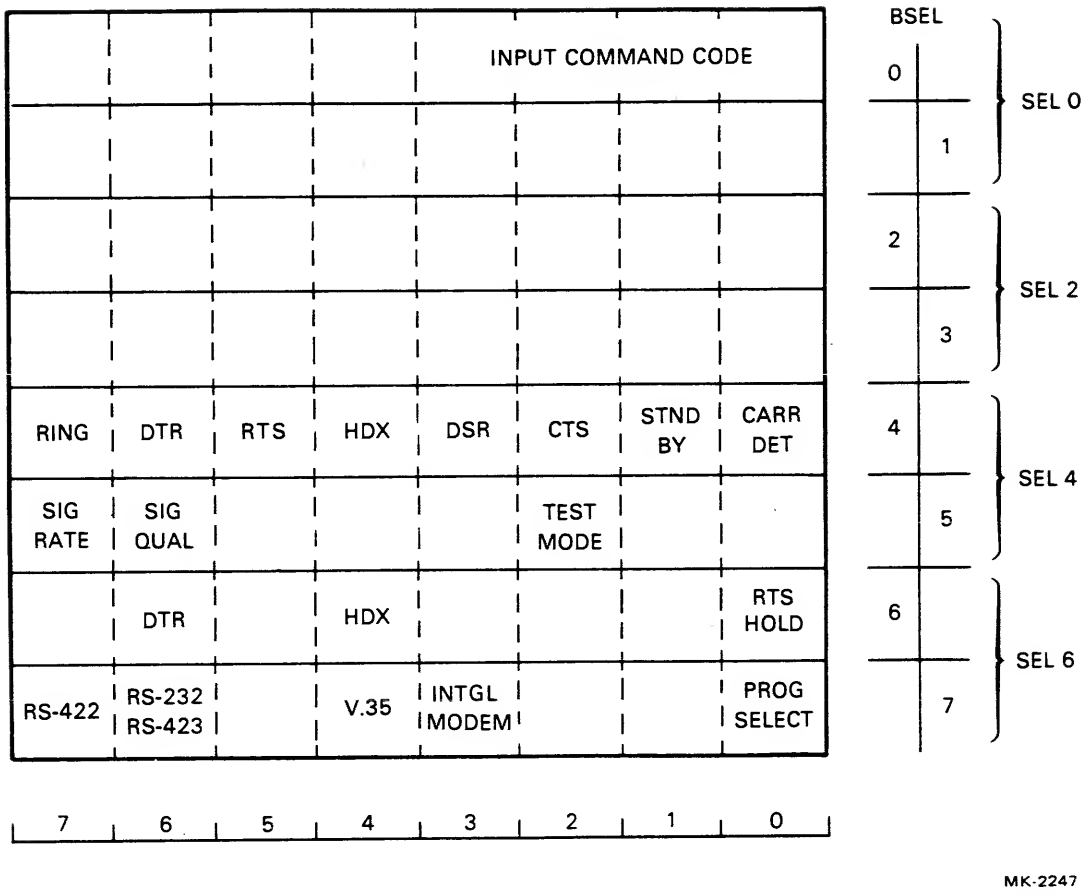


Figure 3-4 Modem Status Read Format

Table 3-4 Modem Status Bit Descriptions

Port	Bit(s)	Name	Description (If Bit is Set)
BSEL 4	0	Carrier	Valid for both the Integral Modem and the modem interfaces. Indicates that the receiver is active.
	1	Standby	References the Standby indication from the modem (refer to EIA specification RS-449).
	2	Clear to Send	This is a reply from the modem indicating that data can be transmitted.
	3	Modem Ready	Indicates that the modem is in service.
	4	Half-Duplex	This indicates that the line unit is set in half-duplex mode.

Table 3-4 Modem Status Bit Descriptions (Cont)

Port	Bit(s)	Name	Description (If Bit is Set)
	5	Request to Send	This indicates that the Universal Synchronous Receiver/Transmitter (USYRT) is ready to start transmitting data as soon as Clear to Send is true.
	6	Data Terminal Ready	A signal from the line unit to the modem indicating the line unit is available and on-line.
	7	Ring	Indicates that the modem has just been dialed up.
BSEL 5	8, 9		Reserved - Bit Condition, don't care.
	10	Test Mode	Indicates that the modem is in the test mode (refer to EIA specifications).
	11-13		Reserved - Bit condition, don't care.
	14	Signal Quality	A signal from the modem that indicates the presence or absence of the carrier. Usually, when this signal is ON it indicates the presence of a carrier and OFF indicates an absence of a carrier.
	15	Signal Rate	A signal from the modem that indicates a data rate. Usually a negative level indicates a lower rate while a positive level indicates a higher rate.
BSEL 6*	0	RTS Hold	This bit is set for FDX at speeds less than 1M b/s in DDCMP normal mode. When set, RTS (EIA CA/CCITT 105) will be held asserted while the communications link is idle (except during error recovery).
	1, 2 & 3		Reserved; Bit condition, don't care.
	4	HDX	When set, indicates that the line unit is set in half-duplex mode.
	5		Reserved; Bit condition, don't care.
	6	DTR	When set indicates that the line unit is available and on-line.

*BSEL 6 contains data written to the modem register by the DMR11, as opposed to SEL 4 which contains what was read.

Table 3-4 Modem Status Bit Descriptions (Cont)

Port	Bit(s)	Name	Description (If Bit is Set)
	7		Reserved; Bit condition, don't care.
BSEL 7 (applies only after Base Table is assigned)	8		Program Selected - Used for diagnostic purposes. When set, the modem interface is defined by other bits in BSEL 7. Used for test purposes when clear.
	9 & 10		Reserved; Bit condition, don't care.
	11		When set, indicates Integral Modem selected.
	12		When set, indicates V.35 interface selected.
	13		Reserved; Bit condition, don't care.
	14		When set, indicates RS-232-C or RS-423-A interface selected.
	15		When set, indicates RS-422-A interface selected.

3.2.4 Output Commands Overview

Output commands provide a means for the DMR11 to report various normal and abnormal (error) conditions concerning the data transfer operation. Two basic commands are provided:

1. Receive or Transmit Buffer Addresss/Character Count Out and
2. Control Out

The Buffer Address/Character Count Out command is used to report a successful, error free, completion of a receive or transmit buffer and indicates the actual number of bytes transferred. This command utilizes both SEL 4 and SEL 6 to identify the address of the completed buffer and the actual character count of the transfer.

The Control Out command is used to report specific conditions concerning the DIGITAL Data Communications Message Protocol (DDCMP), the user program, the hardware, or the modem. Control Out utilizes SEL 6, as shown in Figure 3-5, to inform the user program as to the nature of the report. The various conditions are shown below.

- Error Status

  Identifies the reason for the error condition; that is, errors can be associated with the DDCMP, the user program, modem, or other hardware limitations. In some cases the error condition is non-fatal and normal operations can continue. Other errors are fatal, causing the DMR11 to shut-down.

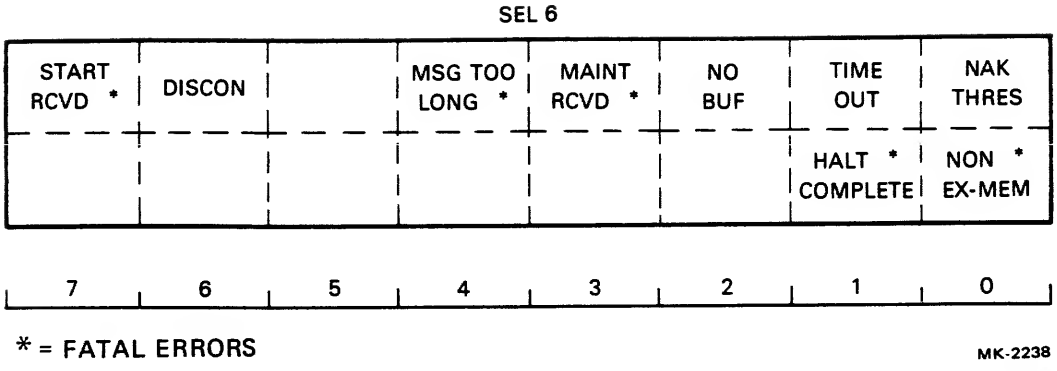


Figure 3-5 Summary of Control Out Status

Detailed bit descriptions of SEL 6 for Control Out are contained in section 3.4.3.

3.2.4.1 Output Command Handshaking

The DMR11 issues output commands in two steps. The data pertinent to the command being issued is loaded into SEL 4 and 6. Once this is complete, the DMR11 sets the Ready Out (RDO) bit and the command code in BSEL 2, and generates an interrupt through vector XX4 if the IEO bit is set. Generally, processing an output command involves the following steps:

- The user program checks for RDO set. This can be done through periodic checking or by waiting for an interrupt, assuming that interrupts are enabled.

NOTE

It is strongely recommended that the output interrupt capability be used to avoid unnecessary delay on the M8207-RA processor when CSRs are constantly scanned.

- To use the output interrupt capability, the user program must set the output interrupt enable bit in BSEL 2 immediately after it detects that Run bit has been set following Master Clear. After Base In, IEO must never be changed unless RDI or RDO is set.

- When a RDO set condition is detected, the user program should read SEL 2, SEL 4, and SEL 6 into three registers or a storage area and clear RDO in BSEL 2. When RDO is cleared, the data port (SEL 4 and 6) will be released for more input or output command processing.

The flow chart in Figure 3-6 illustrates a typical procedure for the user program to implement output command servicing. The example shown is for interrupts enabled. It also demonstrates user requirements to process each command. This procedure is provided as an example only and should not be considered as the only method to implement output command servicing.

3.3 INPUT COMMANDS

This section provides detailed descriptions of each input command. Command formats and data port usages are illustrated and defined in terms of user program execution requirements, command variables, and action taken by the DMR11 in response to the command.

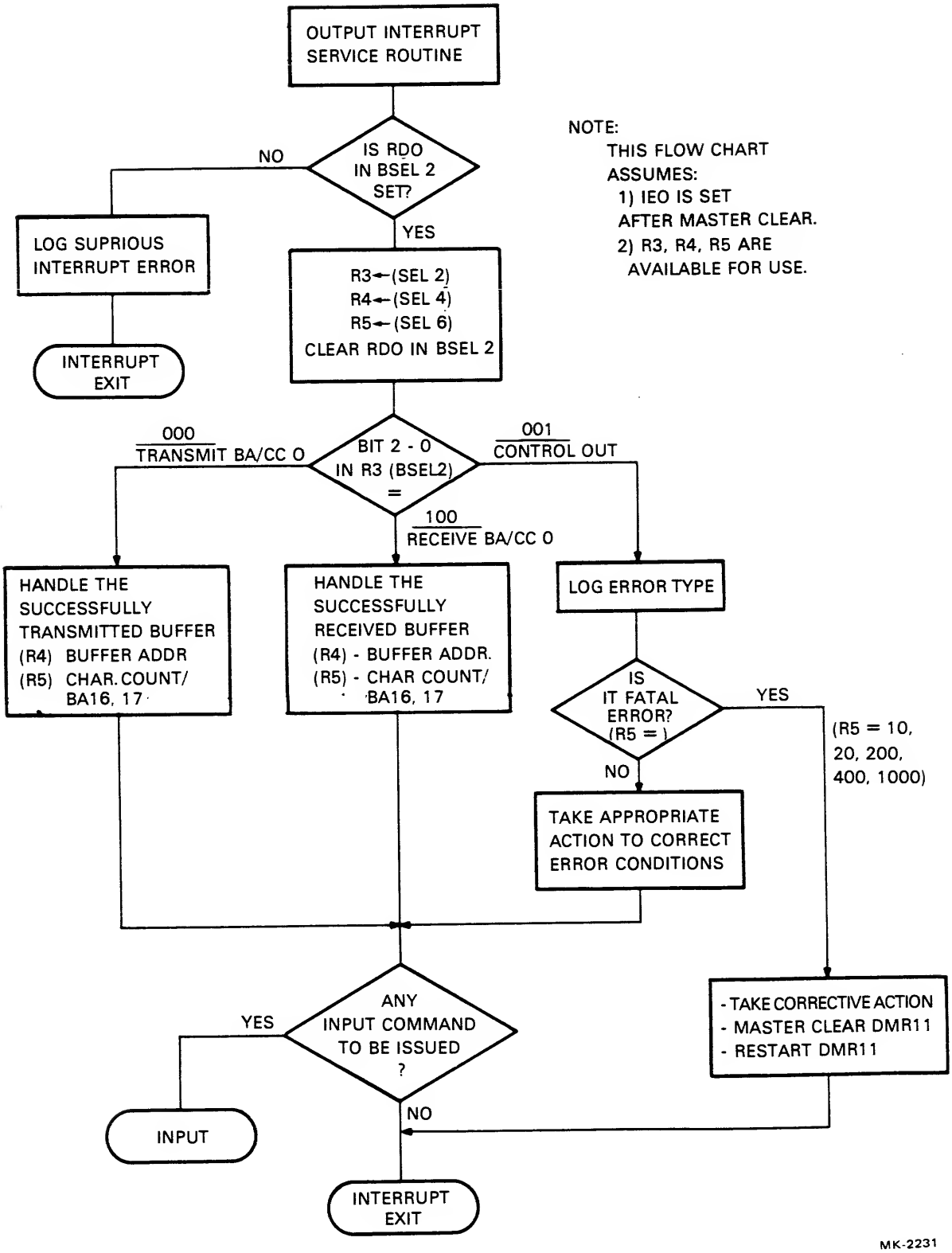


Figure 3-6 Output Command Servicing

3.3.1 Base In

The Base In command is the only command allowed after initialization. It performs two basic functions:

1. Assigns a Base Table to the DMR11 and
2. Implements the Resume feature

The command format for Base In is shown in Figure 3-7. Base In assigns a Base Table of 128_{10} bytes to the DMR11, beginning at the address specified in SEL 4. This table remains assigned to the DMR11 until it is initialized or shut-down by the Halt command.

If the Resume bit (SEL 6, bit 12) is asserted by the user program, the DMR11 immediately reads the contents of the Base Table into its random access memory (RAM). At this time, the DMR11 also examines the Base Table for non-existent memory (NXM). If there is a NXM error, the DMR11 will report the error by Control Out/NXM. For additional material concerning Base In with the Resume feature, refer to section 3.5.2.

NOTE

The user program should not assign the Base Table at an odd address boundary.

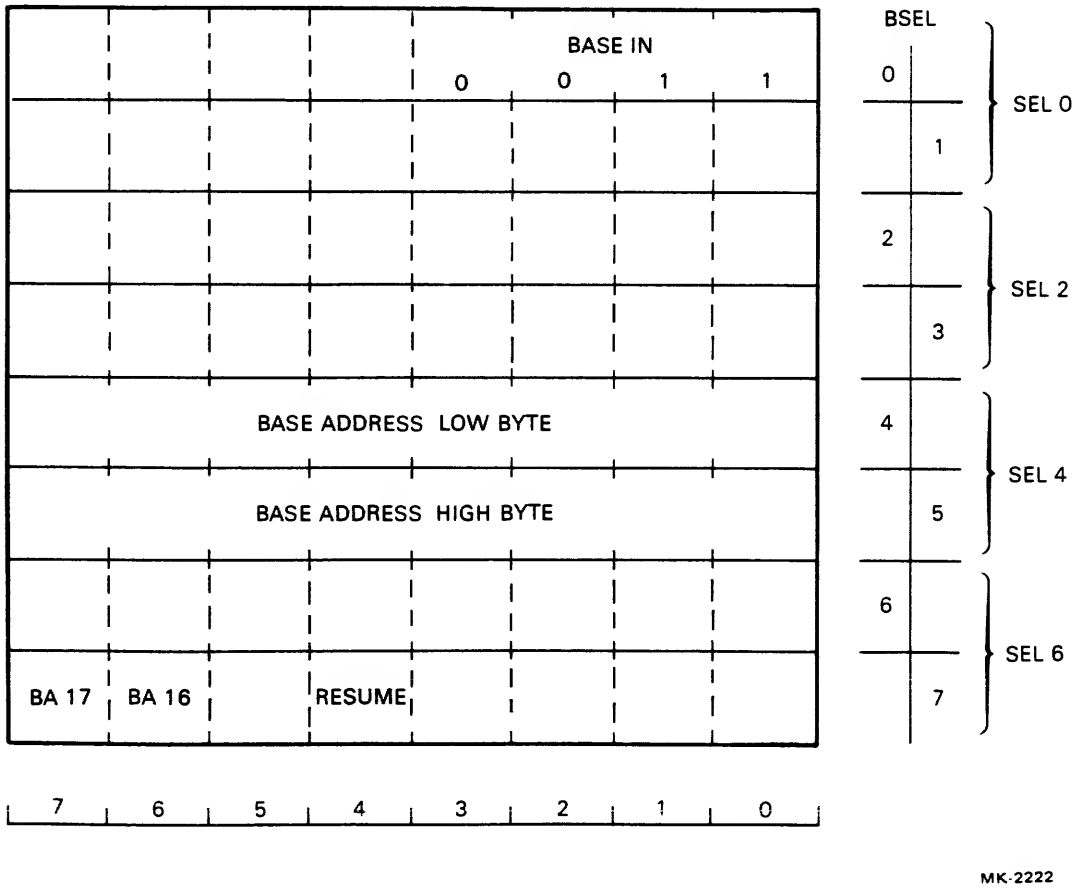


Figure 3-7 Base In Command Format

3.3.2 Control In

This command must be executed following Base In. It provides further definition of the operation by making specific mode selections in BSEL 7. Command In performs three major functions.

- Selects DDCMP Normal or Maintenance Mode,
- Selects half-duplex of full-duplex, and
- Selects the Start Timer

The command format is shown in Figure 3-8. Table 3-5 lists data port (BSEL 7) bit descriptions for this command.

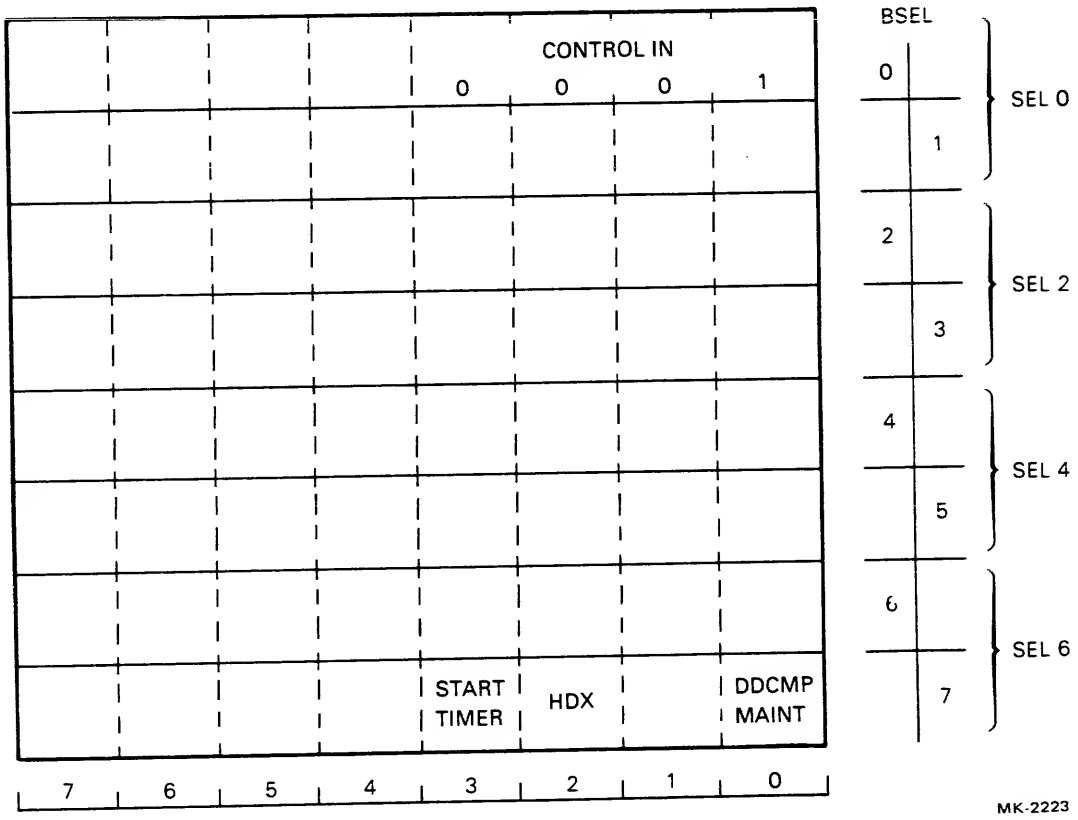


Figure 3-8 Control In Command Format

If selected for DDCMP Normal Mode, the first Control In causes the DMR11 to initiate a protocol start-up sequence and send Start and acknowledge Stack messages. The interval for sending Start messages can be either one or three seconds and is selected by the user program in Bit 3 of BSEL 7. The one second timer interval is the default value.

In full-duplex mode, the timer value selection is not critical because Start message collisions on the line are not possible. In half-duplex mode, however, even though the possibility is slight, Start messages could be issued by both devices at the same time. With identical time intervals, Stack would never occur.

To eliminate this remote possibility, the user program can select the three second timer at one end to offset the interval. In this case, only the first coincident Start message would not return a Stack. The device set at one second will have priority. This condition is illustrated in Figure 3-9.

Table 3-5 Data Port Descriptions with Control In

Port	Bit(s)	Function	Description
BSEL 7 (Write)	0	DDCMP Maintenance	DDCMP Maintenance – When set by the user program, it causes the microprocessor to enter the DDCMP Maintenance Mode. It will remain in this mode until initialized. When this bit is "0" the microprocessor will enter DDCMP Normal Mode.
	2	Half-Duplex	HDX – When set, half-duplex mode is selected. When cleared by the program, full-duplex mode is selected.
	3	Long Start Timer	When set, a three second Start timer is selected; when clear, a one second Start timer is selected (the Start timer is the interval for sending Start/Stack).
	1 & 4-7		Reserved; Bit condition, set to 0.

If selected for DDCMP Maintenance Mode, a special DDCMP message format, the maintenance message, is used for down-line loading, restarting, or otherwise maintaining satellite computer systems. Messages in this format are subject to error checking but are unsequenced, unacknowledged, and not automatically retransmitted by the microprocessor.

To set the DMR11 into Maintenance Mode, the user program must initialize the DMR11, give it a Base In with the Resume bit clear, a Control In with the maintenance bit set, and set the half-duplex bit for HDX or clear for FDX.

In Maintenance Mode the DMR11 provides the following functions:

1. Message framing.
2. Bit error detection - The header and data block check character (BCC) is checked by the DMR11. If the BCC is bad, the message is discarded with no notification given to the user program.
3. Link management - The DMR11 provides proper line turn-around in half-duplex mode.
4. Some errors are recorded in the DMR11's internal RAM memory and are reported to the user program by updating the Base Table.

It is the responsibility of the user program to recover from any error via software time outs, since there is no retransmission attempted in maintenance mode.

3.3.3 Receive Buffer Address/Character Count In (RBA/CCI)

The RBA/CCI allows the user program to assign a receive buffer by giving the DMR11 the starting address of the buffer and the character count in SEL 4 and SEL 6. The DMR11 can accept up to 64 receive buffers.

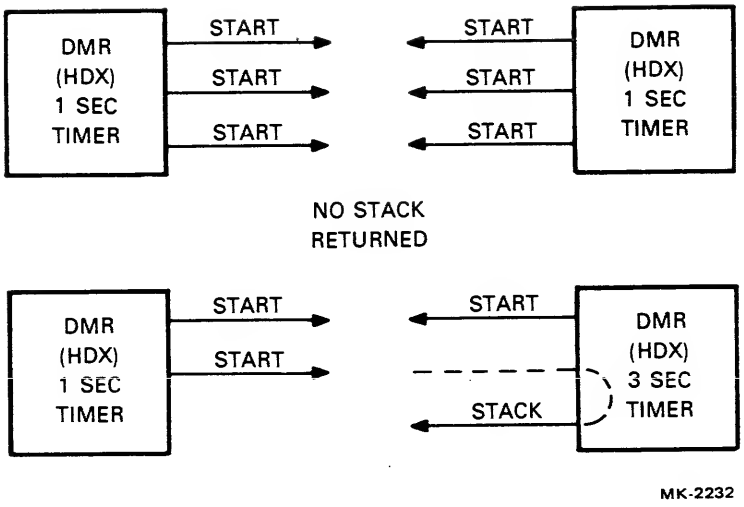


Figure 3-9 Start/Stack Sequence Timer

NOTE

DMC11 can only accept a maximum of 7 buffers.

If the Resume feature is to be used, the maximum number of receive buffers is limited to eight. If the DMR11 has more than eight buffers, it will only save up to eight after Resume. For example, if DMR11 has BUF 1, BUF 2,....BUF 20 after a Shutdown/Resume operation, the DMR11 will only retain BUF 1, BUF 2,....BUF 8. The format for RBA/CCI is shown in Figure 3-10.

The starting address of the receive buffer is contained in SEL 4 and the two most significant bits of SEL 6. The buffer size is contained in the remaining bits of SEL 6. Buffers range from 1 to 16,383 bytes. The buffer size should be limited to a practical size large enough to accommodate the longest message expected. Each buffer corresponds to one DDCMP data message.

NOTE

The user program should give a higher priority to assigning all receive buffers before it assigns any transmit buffers. For example, if seven receive and seven transmit buffers are to be assigned, the program should assign all seven receive buffers before assigning any transmit buffers.

3.3.4 Transmit Buffer Address/Character Count In (TBA/CCI)

The TBA/CCI allows the user program to assign a transmit buffer by giving the DMR11 the starting address of the buffer and the character count in SEL 4 and SEL 6. The DMR11 can accept up to 64 transmit buffers.

NOTE

DMC11 can only accept a maximum of seven buffers.

If the Resume feature is to be used, the maximum number of transmit buffers is limited to eight. If the DMR11 has more than eight buffers, it will only save up to eight after Resume. For example, if DMR11 has BUF 1, BUF 2,....BUF 20 after a Shutdown/Resume operation, the DMR11 will only retain BUF 1, BUF 2,....BUF 8. Buffers range from 1 to 16,383 bytes.

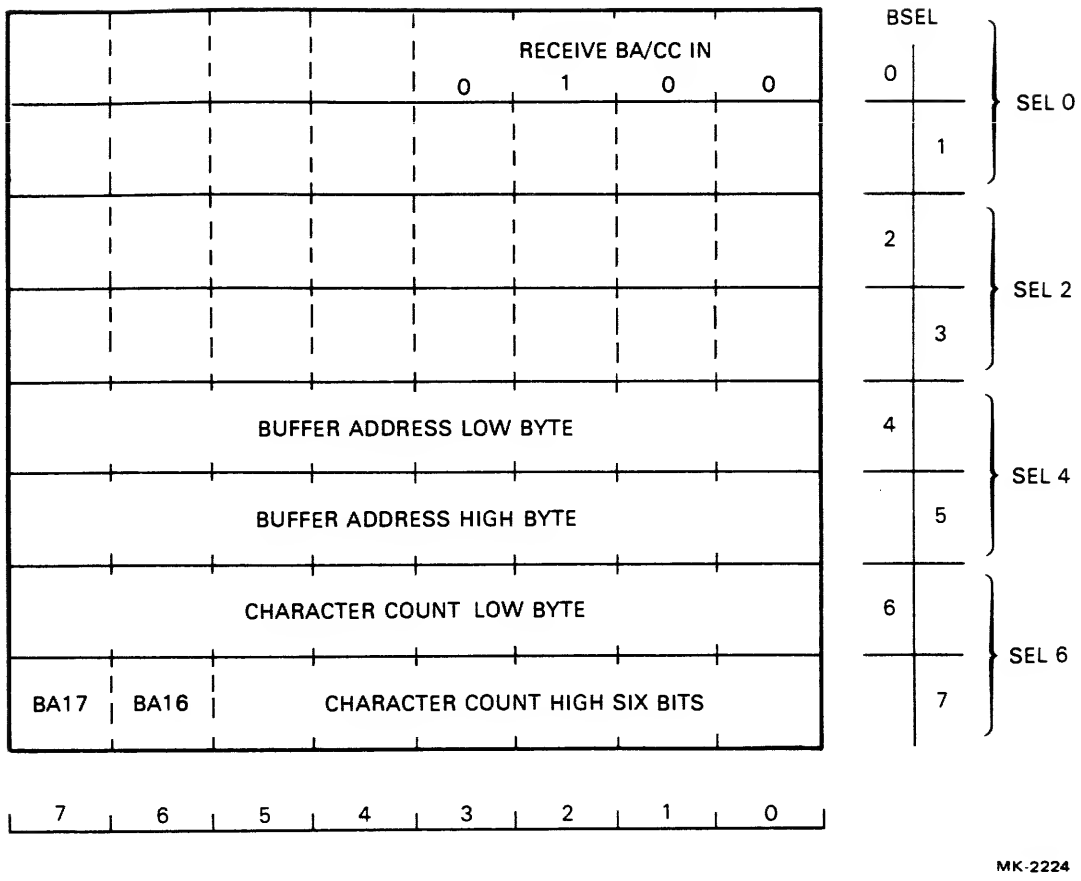


Figure 3-10 Receive Buffer Address/Character Count In Command Format

The maximum size of the transmit buffer is a factor of the line speed and the reply or selection timer value. The time (T) required to transmit each buffer should be less than either the reply timer value (FDX) or the selection timer value (HDX). The user can optimize the buffer size using the following formula:

$$T = \frac{(\text{Character Count} + 20) \times 8}{\text{Line Speed}} \quad \text{or} \quad \text{Character Count} = \frac{(T \times \text{Line Speed})}{8} - 20$$

Where:

T = Seconds (should be less than the 3 second REP/Select Timer)

Line Speed = Bits per second (b/s)

Character Count = Number of bytes

Each buffer corresponds to one DDCMP data message. The format for this command is shown in Figure 3-11.

3.3.5 Halt Request Command

The Halt Request command format is shown in Figure 3-12.

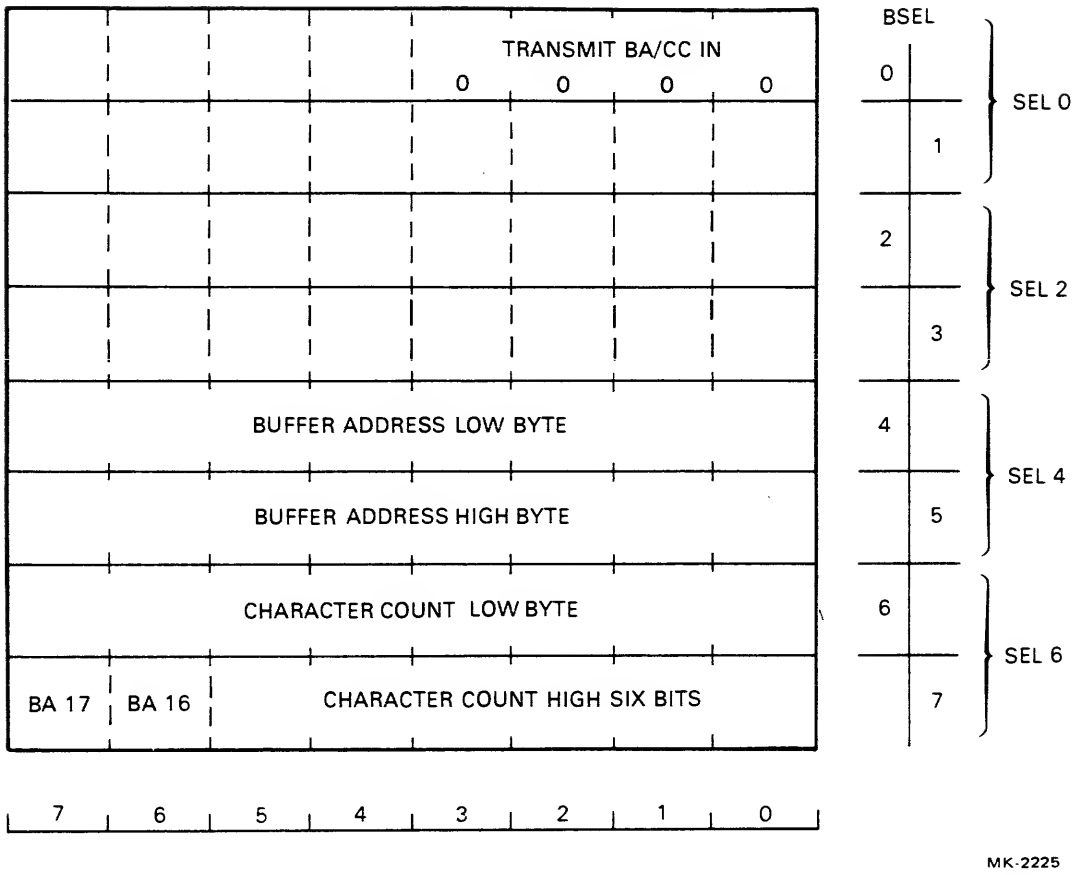


Figure 3-11 Transmit Buffer Address/Character Count In Command Format

Halt Request allows the user to request a controlled DMR11 shut down; that is, in the proper order. Halt Request is the only formal method used to shut down the DMR.

CAUTION

If the Halt Request command is issued with outstanding transmit buffers, the DMR11 will abort a transmission in progress.

The DMR11 shutdown sequence is as follows:

1. Clear data terminal ready (DTR). This condition is performed only when a Halt Request command is issued. It does not occur during a fatal error shut-down.
2. Return all queued up Control Outs.
3. Dump the Base Table to local CPU Memory. The DMR11 will wait up to three seconds for data set ready (DSR) to clear, before issuing Control Out with Halt Complete.
4. Initialize the scratch pads and RAM location 0-400, and reset the M8203 line unit.

   Data ports are not used for the Halt Request command.

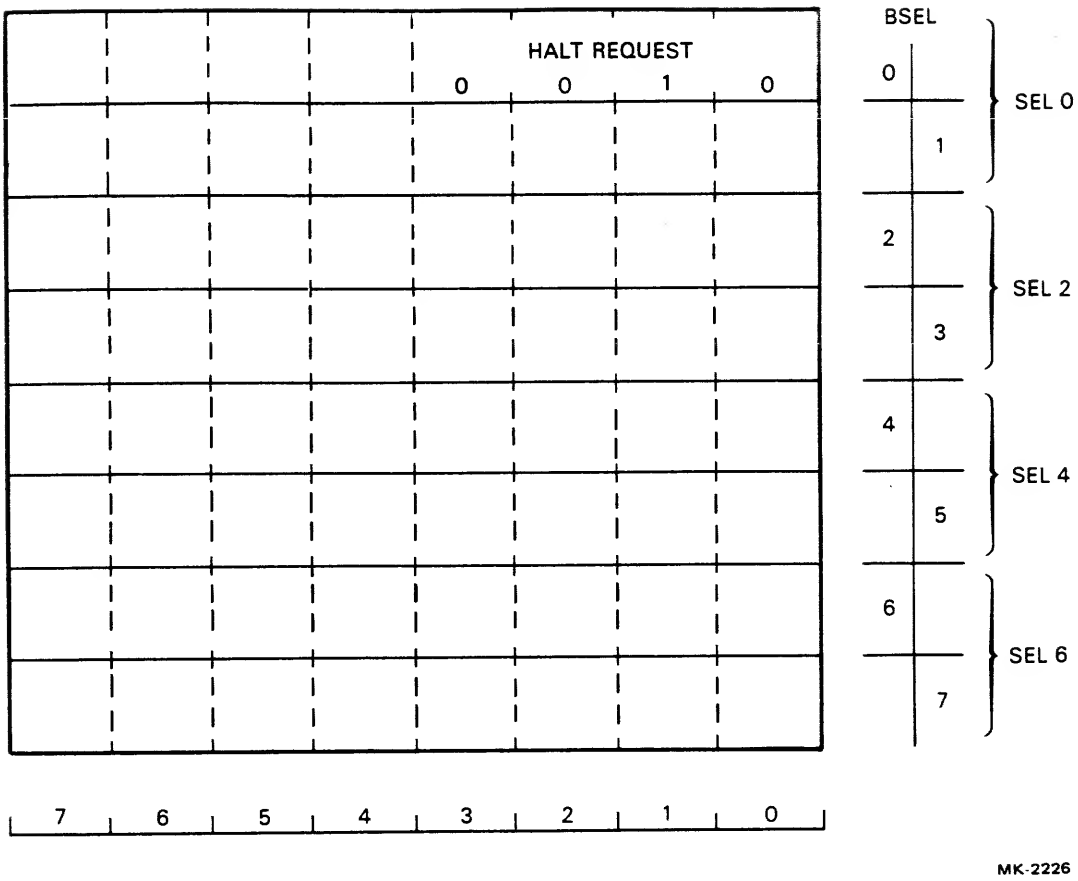


Figure 3-12 Halt Request Command Format

3.4 OUTPUT COMMANDS

Output Commands provide a means for the DMR11 to report various normal or abnormal (error) conditions pertaining to the data transfer process. There are two basic commands:

1. Buffer Address/Character Count Out, which is further categorized into receive or transmit buffers, and

2. Control Out.

The Buffer Address/Character Count Out command is used to report normal transfer completions to the user program. Control Out is used to report abnormal (error) conditions. In either case, if the Interrupt Enable Out (IEO) bit is set, the DMR11 will interrupt the CPU to vector XX4. If the IEO bit is disabled (0), the user program, by sensing Ready Out (RDO), assumes the responsibility of recognizing that an output command is pending.

When the output command is complete, the user program can execute an Input Command. However, the DMR11 will not recognize an input request until output command servicing is completed.

3.4.1 Receive Buffer Address/Character Count Out (RBA/CCO)

This command is used by the DMR11 to report successful completions of receive buffers to the user program. The format for this command is shown in Figure 3-13.

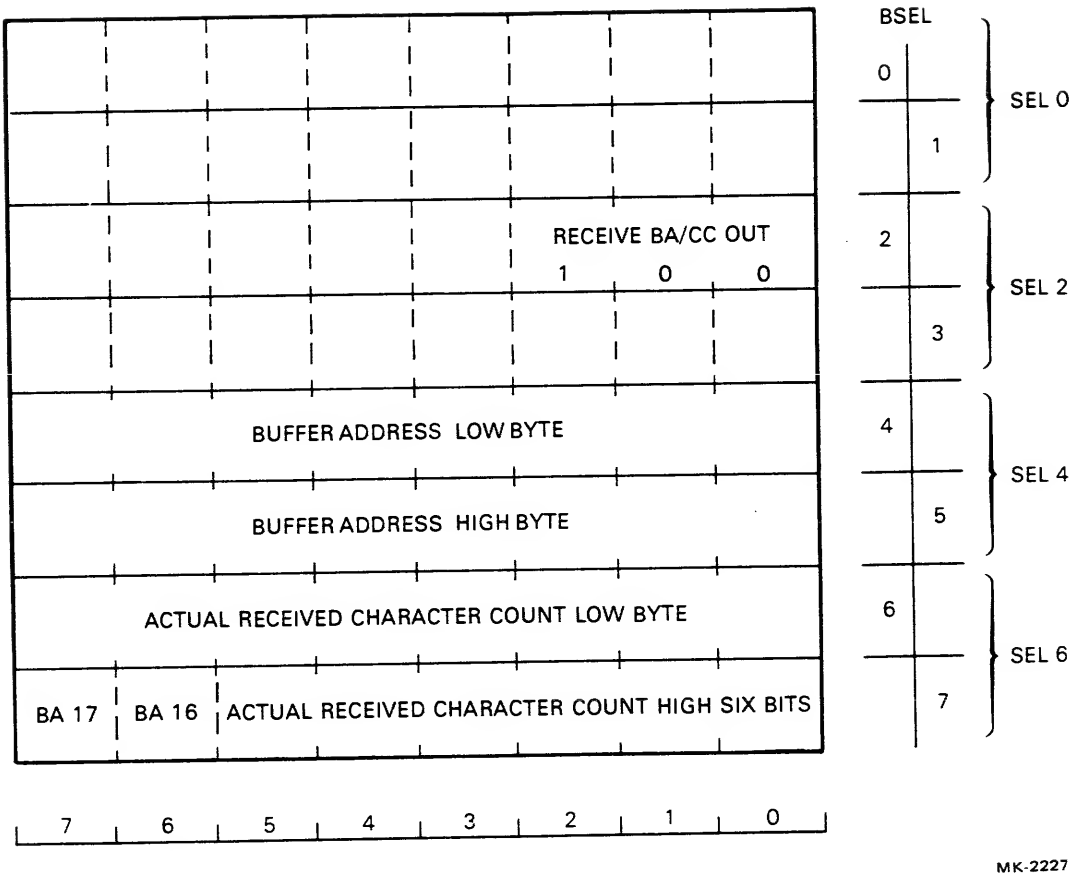


Figure 3-13 Receive Buffer Address/Character Count Out Command Format

The address of the completed buffer is contained in SEL 4 and the two most significant bits (MSB) of SEL 6, while the actual received character count is contained in the remaining bits of SEL 6.

In the normal DDCMP mode, this command indicates that:

- Cyclic redundancy checks (CRC) are good,
- The sequence number is correct,
- The protocol requirement checks are good, and
- The data is stored in memory (DMAed).

In DDCMP Maintenance mode, the following is valid:

- CRCs are good,
- Protocol requirement checks are good,
- Data is stored in memory (DMAed).

3.4.2 Transmit Buffer Address/Character Count Out (TBA/CCO)

This command is used by the DMR11 to report successful completions of transmit buffers to the user program. The address of the completed buffer and character count are contained in SEL 4 and SEL 6.

In normal DDCMP mode, this command indicates:

- The data was successfully transmitted and
- An acknowledgement for that message has been received from the remote station.

This command when issued in DDCMP Maintenance mode only indicates:

- Data was transmitted.

Figure 3-14 illustrates the format for this command.

3.4.3 Control Out

The DMR11 informs the user program of unusual or error conditions involving the microprocessor hardware, user program, physical link, or remote station by means of the Control Out command.

Some error conditions are non-fatal; that is, after taking the appropriate action, such as assigning more buffers for No Buffer Available, normal data transfer operations may continue. Other error conditions are fatal, causing the DMR11 to shut down. Fatal errors require the user program to reinitialize the DMR11. The format for this command is shown in Figure 3-15.

The port (SEL 6) bit descriptions for Control Out are listed in Table 3-6.

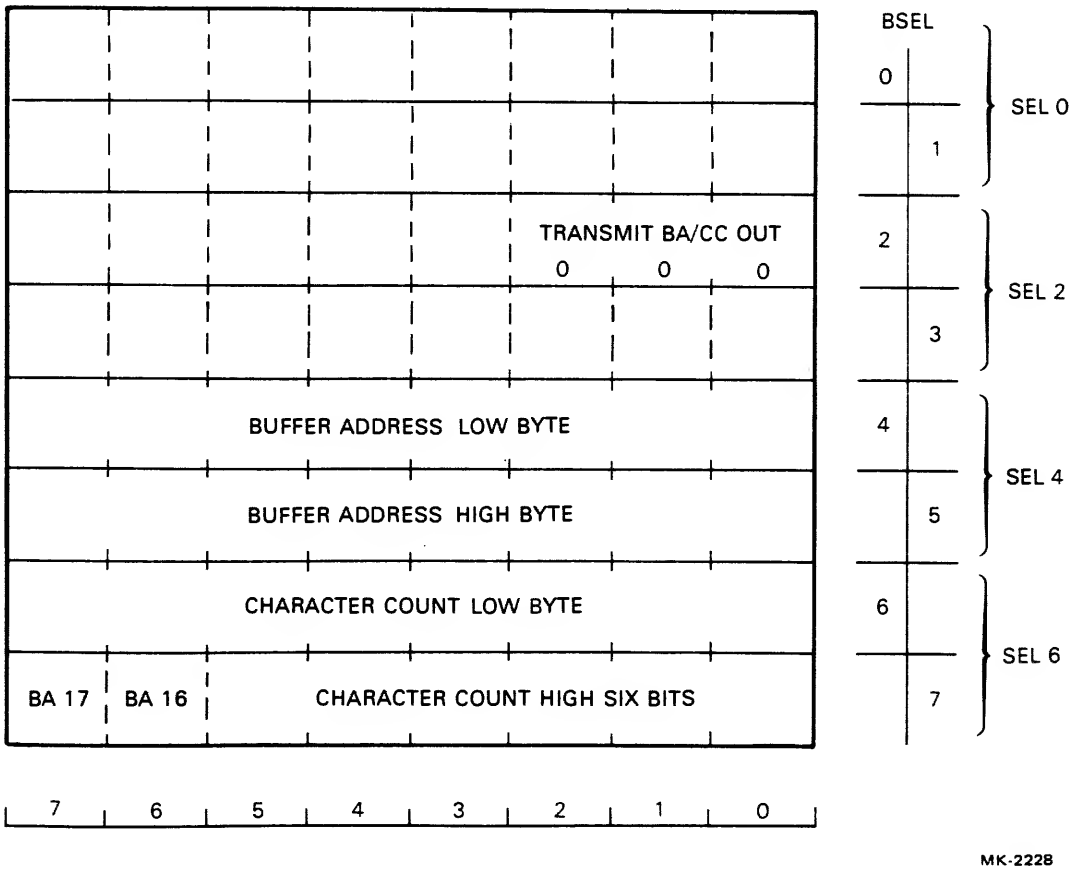


Figure 3-14 Transmit Buffer Address/Character Count Out Command Format

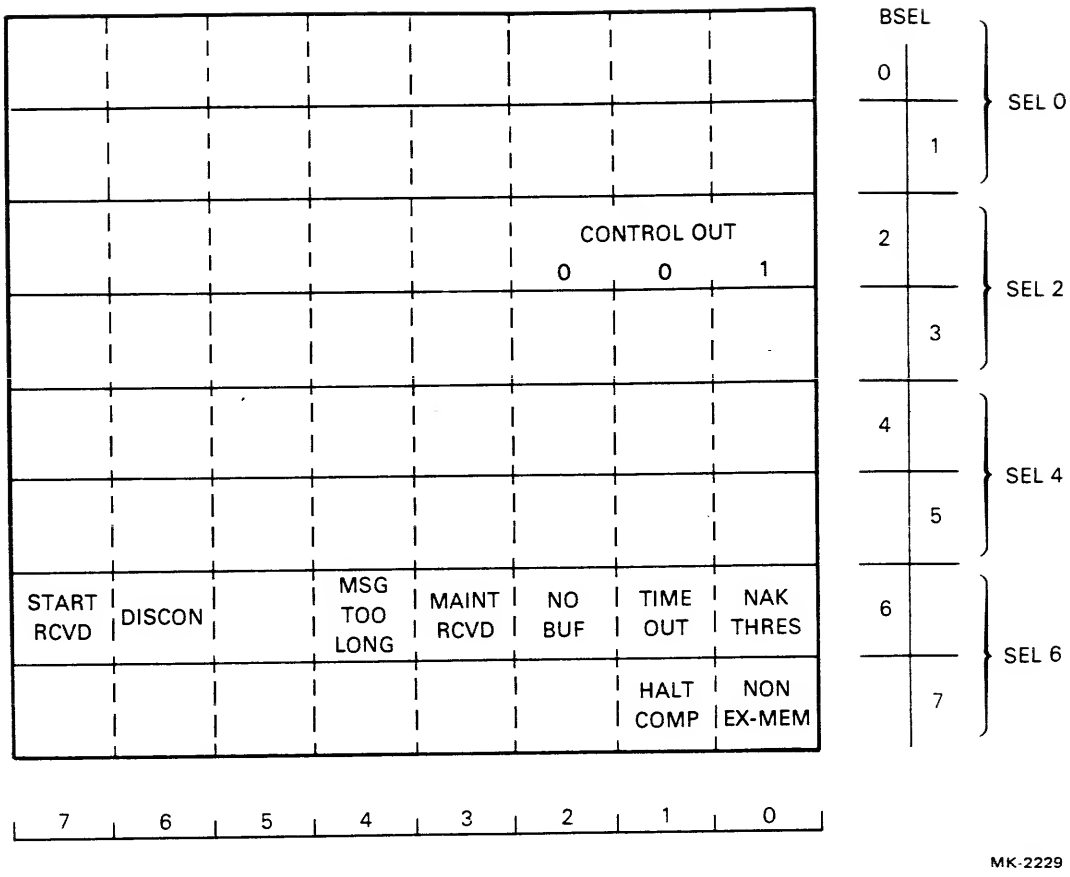


Figure 3-15 Control Out Command Format

3.5 PROGRAMMING TECHNIQUES

This section provides various recommendations and considerations necessary for the user program to properly interface to the DMR11 microprogram.

These considerations are further defined in terms of DDCMP Normal Mode and DDCMP Maintenance Mode. The state diagram in Figure 3-16 shows the relationship of each command to the DDCMP states.

Specific areas for consideration are summarized below and are explained in detail in subsequent paragraphs.

- Proper command sequence
- Execution of input commands with the Resume feature
- How to distinguish DMR11 from DMC11
- Implementation of DDCMP Maintenance Mode
- Execution of remote load detect
- Error detection

Table 3-6 Data Port Bit Descriptions With Control Out

SEL 6 Bit	Name	Status Type	Description
0	NAK Threshold	Error/Non-Fatal (Protocol)	This error is reported when persistent line errors occur, resulting in protocol NAK to be sent or received. When consecutive NAK transmissions or NAK receptions occur, they are counted in their respective threshold counter. When the threshold value of seven is reached, this error is reported. Each threshold counter is cleared when the threshold is reached or when the operation it is monitoring is performed correctly.
1	Time Out	Error/Non-Fatal (Protocol)	When consecutive REP transmissions occur, they are counted in the threshold counter. This error is reported when the threshold value of seven is reached. Each threshold counter is cleared when the threshold value is reached or when the operation it is monitoring is correctly performed.
2	No Buffer	Error/Non-Fatal (User Program)	This error is reported for the following conditions: DMR11 has received seven NAKs because of No Receive Buffer Available at the remote end. There were seven attempts to receive a message with No Buffer Available.
3	Maintenace Received	Error Fatal (Protocol)	A DDCMP Maintenance message format was received while the DMR11 was in DDCMP Run/Start or ASTRT mode. The message causing this condition is lost and the DMR11 is forced to shut down.
4	Message Too Long	Error Fatal (Program)	A received message or transmitted message is larger than the assigned buffer (incluuding maintenance messages). The DMR11 will have shut down by the time this error is reported.
5	Not Used		
6	Disconnect	Error Non-Fatal (Modem)	Indicates that an unexpected drop in DSR (EIA Interface CCITT-107) was detected.

NOTE

On applications using a switched network via dial-up modems, the ON-to-OFF transition of DSR could indicate that the connection has been terminated and a redial or call set up may be required.

Table 3-6 Data Port Bit Descriptions With Control Out (Cont)

SEL 6 Bit	Name	Status Type	Description
7	Start Received	Error Fatal (Protocol)	A protocol Start message was received while the DMR11 was in the DDCMP Run state. The DMR11 will complete shut-down by the time this error is reported. This error is not reported when the DMR11 is in DDCMP Maintenance Mode.
8	Non-Existent Memory (NXM	Error Fatal (Program/ Hardware)	A non-existent memory (UNIBUS address time out) condition has occurred on a receive or transmit data operation, or a Base Table update/read operation. The DMR11 has completed the shut-down by the time this error is reported.
9	Halt Complete		This condition is reported following completion of the Halt Request Command or programming error; that is, a character count of zero on Transmit or Receive BA/CC In, or assigning Control In or BA/CC In before Base In. Refer to section 3.3.5 for the proper shutdown sequence.
10-15	Not Used		Reserved.

3.5.1 Input Command Sequence

The sequence in which the user program issues input commands is critical. The following identifies the proper sequences. The command sequence is listed in Table 3-7. They are shown in the correct order of program execution.

Initialization is the first function that the program must perform. This action is required to reset both the DMR11 hardware and firmware to the initialized (operational) state.

Base In is the only command that the user can issue following initialization. Any other commands issued before Base In will cause a procedure error, resulting in a DMR11 shut-down. This will require the program to reinitialize the DMR11.

Control In should be issued following Base In. After issuing Control In, the user program can assign either receive or transmit buffers to the DMR11. The sequence of issuing one or the other is not critical, however, the program should give priority to assigning all receive buffers before any transmit buffers. Halt Request can be issued at any time.

3.5.2 Base In Command with Resume Feature

The Resume feature can be implemented during a Base In by the program setting SEL 6 bit 12.

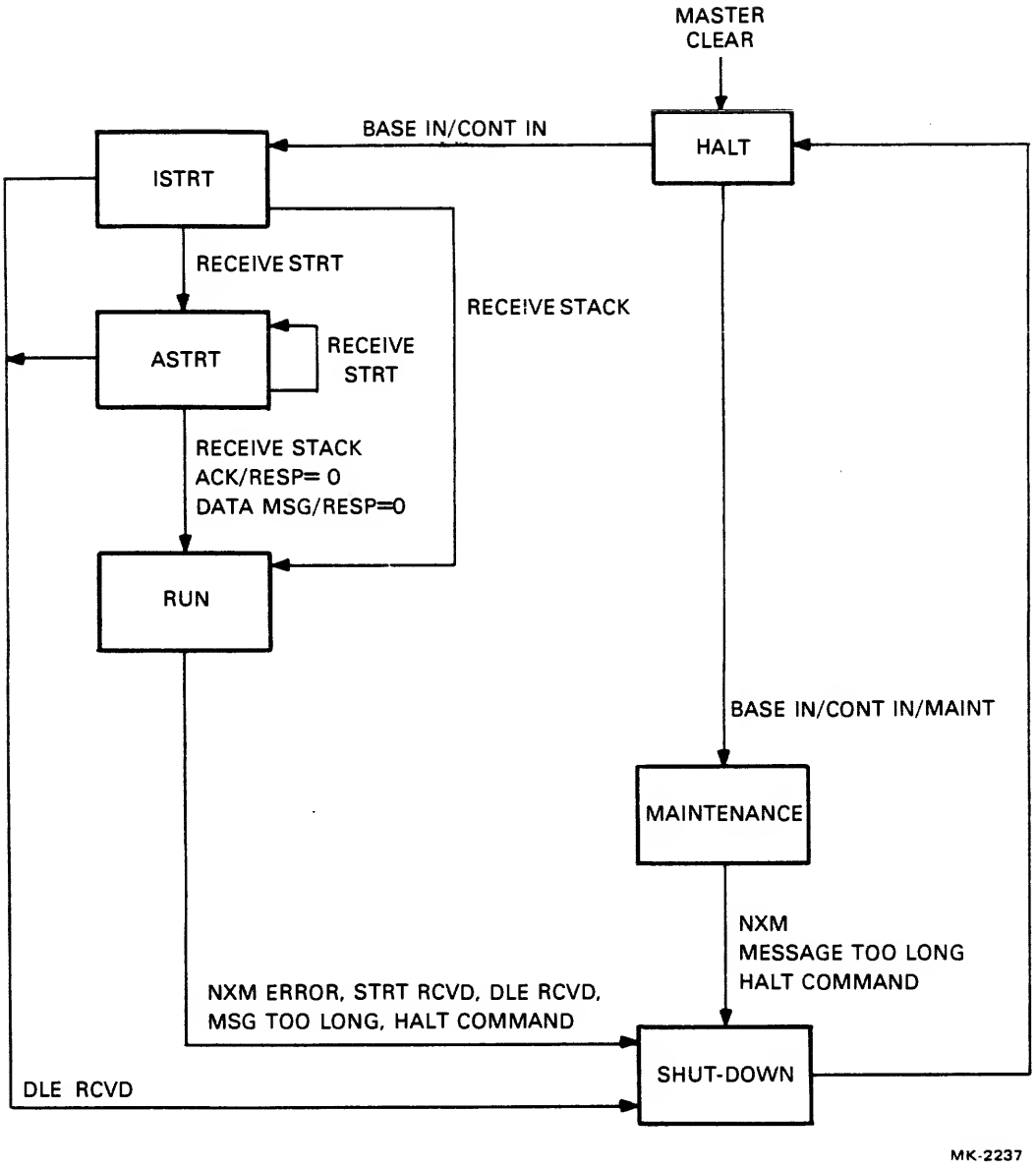


Figure 3-16 DMR11 Protocol State Diagram

The proper command sequence to implement a shut-down and then resume, is as follows:

Input Commands

Halt Request	;shutdown DMR11
Master Clear	;optional (initialized internally by Halt Request)
Base in with Resume set	;resume DMR11
Control In	;To select half-duplex or full-duplex

Table 3-7 DMR11 Command Sequence

Command	Description
Initialization	Master Clears the DMR11 and places it in the operational state.
Base In	Only command allowed after Master Clear. Assigns the Base Table to the DMR11 and prepares for protocol startup.
Control In	Sets DMR11 in either half-duplex or fullduplex mode and either DDCMP Normal (Run) or Maintenance Mode. Also establishes a one or three second Start timer.
Buffer Address/ Character Count In	Assigns receive or transmit buffers. Can assign up to 64 buffers. All receive buffers should be assigned first.
Halt Request	The Halt Request command can be issued by the user program at any time to formally shut down the DMR11.

The Resume feature causes the DMR11 to read the Base table content from the CPU memory and store that data in the DMR11 RAM. This information should be the updated Base Table resulting from the previous shut-down. The information contained in the Base Table will determine whether the DMR11 will Resume operation in the Run, ISTRT, ASTRT or Maintenance State; that is, protocol start up is not required. However, if the remote end has abandoned the process due to protocol time out, it will be necessary to reinitialize.

Buffers assigned to the DMR11 prior to shut-down (up to a maximum of eight receive and eight transmit buffers) will still be assigned when the operation resumes. If there are more than eight outstanding receive or transmit buffers, they will be lost.

NOTE

1. **During shut-down and subsequent Base In with Resume, the Base Table must NOT be altered. If modified, the DMR11 could resume in an undefined state.**

2. **To use this feature, the number of transmit or receive buffers must be less than eight each.**

3. **Whenever the Base Table is written to or read from main memory, resulting from a shut-down or Resume operation, 64 back to back DMAs (5-10 microseconds apart) are execued to transfer the Base Table. Therefore the user must be aware of the effect of the high rate of DMAs on the rest of the system.**

3.5.3 Distinguishing DMR11 from DMC11

If the user program needs to determine if it is interfacing with a DMC11 or a DMR11. The user program can execute the procedure listed below as part of the initialization sequence.

1. Load any number (except 1_8, 2_8, 100_8 or 200_8) into BSEL 3,
2. Set Master Clear bit (with or without microdiagnostics enabled),
3. Wait for the RUN bit (maximum of 6.4 ms), and
4. Check BSEL 3.

   The unit is a DMR11 if BSEL 3 contains either 1_8, 2_8, 100_8, or 200_8.

   NOTE

   If the microdiagnostic is disabled, BSEL 3 will contain 100_8 (Test Inhibited). If enabled, BSEL 3 will contain 1_8, 2_8, or 200_8.

   The unit is a DMC11 if BSEL 3 contains the same number that was written in step 1.

3.5.4 DDCMP Maintenance Mode Operation

Maintenance Mode provides the mechanism to implement down-line program loading or restarting/maintaining satellite computer systems via remote load detect (RLD). In this mode, a special message format (maintenance message) is used to execute this feature. Messages in this format are subject to error checking but are unsequenced (not numbered), unacknowledged, and not automatically retransmitted by the microprocessor. Because of this, it is necessary for the user program to recover from any error conditions by utilizing time outs to retransmit the message.

To enter the DDCMP Maintenance Mode, the DMR11 must be initialized and issue a Base In with the Resume bit cleared, followed by the Control In with the Maintenance bit (SEL 6, bit 8) set.

3.5.4.1 Data Transfer – Once in DDCMP maintenance mode, maintenance messages can be sent and received like data messages. On transmission, the data portion of the message is taken from the assigned buffer with the DMR11 generating the header and CRCs. On reception, only the data portion is placed in the available assigned buffer. Messages not in DDCMP maintenance format, having incorrect CRCs or no receive buffers are simply discarded.

When operating in conformance with MOP, the DMR11 must be operated in a single buffered manner, causing a line turnaround after each message is transmitted. When a host computer wishes to restart a satellite computer system, it must send the appropriate MOP messages as described in section 3.5.4.2.

3.5.4.2 Unattended System Control – Unattended system control (down-line load/remote load detect) is accomplished using the maintenance operation protocol (MOP), version 2.0. There are two basic considerations when using MOP: down-line load (originating station) to remote end and remote (boot station) request for down-line load.

The Enter MOP Mode message is used to control an unattended satellite system. This message, together with the appropriately configured hardware, causes the DMR11 to stop current operations, forcing the computer to transfer control to a resident MOP program or bootstrap.

Whenever the microprocessor is running, it constantly scans the line for a DDCMP maintenace message (DLE) containing an Enter MOP Mode data field.

The data portion of this message contains five bytes. The first byte contains the number code six. The remaining four bytes contain the password, which must match the password assigned to the line unit. All four passwords must be the same.

In order to execute down-line load to the remote station, the following conditions must be true:

1. The password Switch Pack (E134 on the line unit) is NOT set to 377_8.
2. All four passwords in the Enter MOP Mode message match the password selected by Switch Pack E134 on the M8203 line unit (except 377).
3. The data CRC for the ENTER MOP message is good.

Once these conditions are satisfied, the DMR11 will write via direct memory access (DMA) 173XXX into memory location 24 and zero to location 26 followed by pulling AC LO to initiate a power up recovery. The power up recovery causes the CPU to transfer control to a primary MOP program residing in a boot module such as the M9312 with the DECNET boot ROM at location 173XXX. The designation XXX is the content of the boot offset which is selected by the offset Switch Pack E121 on the M8203 line unit. (switches 1-8).

If any of the three conditions are not satisfied, the DMR11 will treat the Enter MOP mode message as specified in Table 3-8.

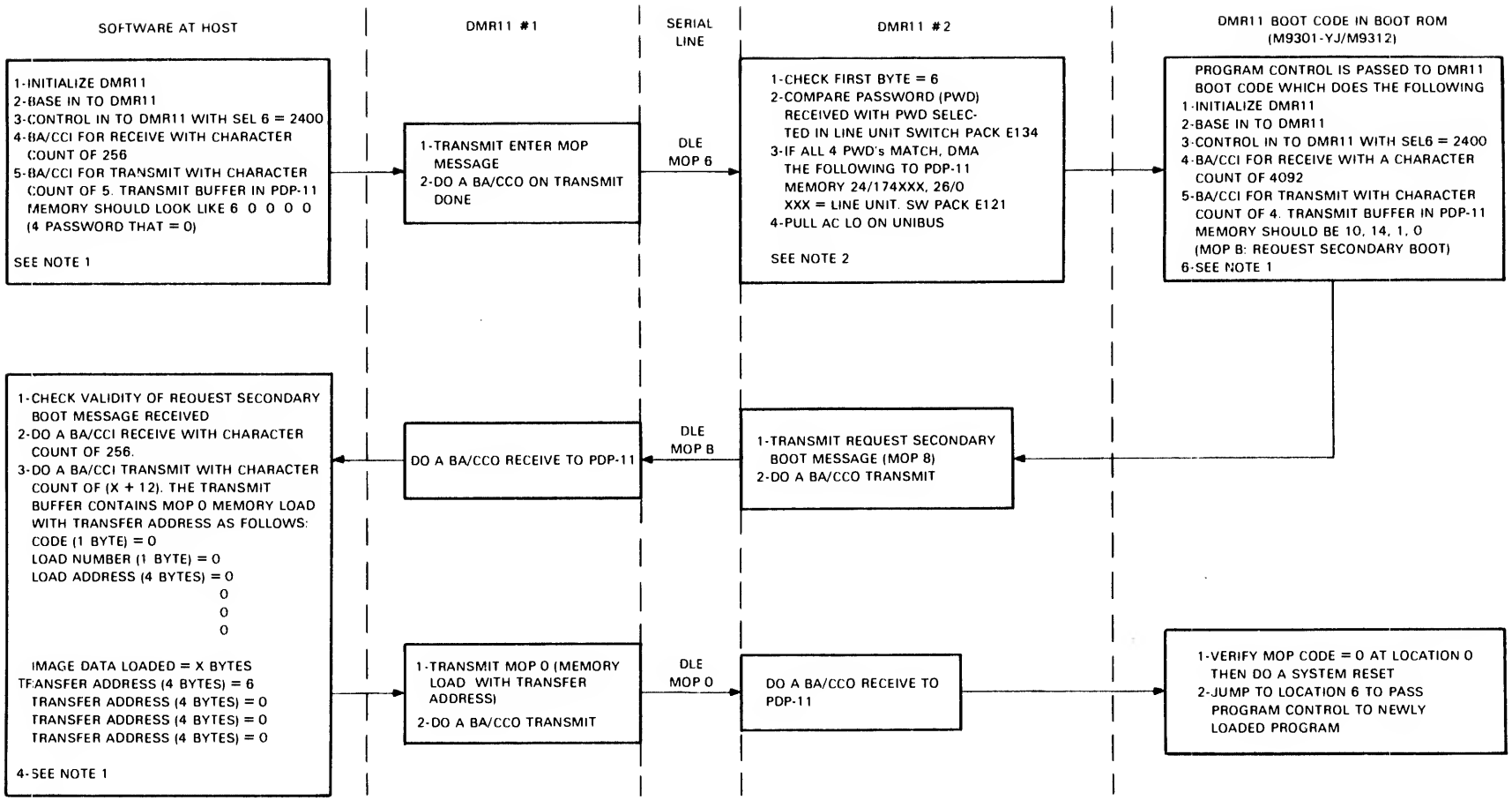
Figure 3-17 illustrates the procedure for remote load detect and the required handshakes to execute this feature. This procedure assumes that the remote device is configured for the appropriate password and offset to implement the bootstrap feature. Appendix E provides a detailed description for executing and testing the bootstrap.

Table 3-8 Invalid Enter MOP Message Response

Condition	Action
DMR11 in Halt or Initialized mode	No action taken.
DMR11 in Run, ISTART or ASTART mode	DMR11 will enter the Halt state and notify the program that a maintenance message (DLE) was received.
DMR11 in Maintenance Mode	If a receive buffer is available and the message contains a CRC error, the message will be discarded and the error counter incremented.

3.6 BASE TABLE COUNTERS

After Base In and Control In are issued by the software, DMR11 will periodically update the internal counters from its RAM location 2 through 42 (see Figure 3-18) to the Base Table assigned. These cumulative error counters start at 0 and wrap around back to 0 when the maximum count is reached. These counters are updated approximately every second.



NOTES:

1) IN DDCMP MAINTENANCE, THERE IS NO RETRANSMISSION; BA/CCO FOR A TRANSMIT OPERATION DOES NOT ASSURE SUCCESSFUL RECEPTION AT THE REMOTE END. THE SOFTWARE MUST KEEP A REPLY TIMER OF 3 SECONDS TO RETRANSMIT THE MESSAGE WHEN NO REPLY IS RECEIVED WITHIN THAT TIME

2) XXX MUST BE THE OFFSET FROM 173000 OF THE DMR11 BOOT CODE IN M9301-YJ/M9312

MK 2246

Figure 3-17 Down-Line Load Procedure to Remote Station

```
BASE
TABLE
ADDRESS                          BASE TABLE ALLOCATION


        ;NAME
        ;----
        ;
000000  UPINDX  ;! BASE TABLE UPDATE INDEX POINTER
000001  UPLMT   ;! BASE TABLE UDPATE LIMIT
000002  BASTBL  ;# BEGINNING OF BASE TABLE DATA          (ALWAYS = 000)

000003  NRNBF   ;@ NAKS RCVD - BUFFER TEMP UNAVAILABLE (REASON =  8.)
000004  NRHCE   ;@ NAKS RCVD - HEADER BCC ERROR         (REASON =  1.)
000005  NRDCE   ;@ NAKS RCVD - DATA BCC ERROR           (REASON =  2.)

                ; ** --- IN DDCMP MAINTENANCE MODE THESE
                ;         IN-BOUND ERRORS ARE RECORDED BUT
                ;        NO NAKS ARE SENT.

000006  NSNBF   ;@ NAKS SENT - BUFFER TEMP. UNAVAILABLE          (REASON =  8.)  **
000007  NSHCE   ;@ NAKS SENT - HEADER BCC ERROR         (REASON =  1.)  **
000010  NSDCE   ;@ NAKS SENT - DATA BCC ERROR           (REASON =  2.)  **

000011  RST     ;@ REPS SENT - CUMUL REP SENT.
000012  RRCV    ;@ REPS RCVD - CUMUL REP RCVD.

000013  NRREP   ;# NAKS RCVD - REP RESPONSE             (REASON =  3.)
000014  NRROV   ;# NAKS RCVD - RCV OVERRUN              (REASON =  9.)
000015  NRHFM   ;# NAKS RCVD - MSG HDR FORMAT           (REASON = 17.)
000016  NRMTL   ;# NAKS RCVD - MSG TOO LONG             (REASON = 16.)

000017  NSREP   ;# NAKS SENT - REP RESPONSE             (REASON =  3.)
000020  NSROV   ;# NAKS SENT - RCV OVERRUN              (REASON =  9.)  **
000021  NSHFM   ;# NAKS SENT - MSG HDR FORMAT           (REASON = 17.)  **

000022  XUNDR   ;# XMIT UNDERRUN COUNT.

000023  CFAIL   ;# CALL SET UP FAILURE COUNT.

000024  CTSCNT  ;# CTS FAILURE COUNT.

000025  CDLCNT  ;# CARRIER DETECT LOST COUNT
                ;# (WHILE RECEIVING)

000026  RCVIDL  ;# RECEIVER INACTIVE COUNT.

000027  STRCNT  ;# STREAMING TIME-OUT COUNTER

000030  XMBYT   ;# TOTAL NUMBER OF BYTES TRANSMITTED.
                ;# (INCLUDING RETRANSMISSION, 32 BIT
                ;# COUNTER)
000034  RCBYT   ;# TOTAL OF BYTES RECEIVED. (NOT
                ;# INCLUDING DUPLICATE OR OUT OF
                ;# SEQUENCE, 32 BIT COUNTER)

000040  ICSEL   ;# INCOMPLETE SELECTION COUNTER
000041  NRSEL   ;# NO REPLY TO SELECTION COUNTER
```

Figure 3-18 DMR11 Base Table Error Counters

3.7 MODEM CONTROL

There are two levels of modem control available in the DMR11. The first level is provided by the M8203 hardware and the second is provided by the DMR11 microcode.

3.7.1 Modem Control Implemented in M8203

3.7.1.1 Modem Ready Lockout of RTS – Bit 3 of line unit Register 13 is data mode (modem ready) or data set ready (Circuit EIA CC/CCITT-107). Unless modem ready is asserted by the modem, M8203 will not present request to send (Circuit EIA CA/CCITT-105) to the modem.

3.7.1.2 Half Duplex Mode – Bit 4 of line unit Register 13 is the half-duplex bit; if set, it indicates that the line unit is set in the half-duplex mode. In half-duplex mode, there is hardware interlock to prevent the line unit from transmitting and receiving simultaneously. While the receiver is actively receiving or carrier detect is asserted, the data loaded into the transmit silo will not be loaded into the USYRT for transmission and therefore RTS will not be presented to the modem. Similarly, while the transmitter is transmitting, the receiver is disabled from receiving data.

NOTE

This hardware interlock will prevent the M8203 line unit from being used in half-duplex mode on a full-duplex modem, with the continuous carrier option installed.

3.7.2 Modem Control Implemented in DMR11 Microprogram

3.7.2.1 Auto-Answer – When the DMR11 is installed on a switched line, Switch Pack E134 switch 9 should be placed in the OFF position. This enables the DMR11 to monitor RI and DSR, utilizing a 20 second timer to answer and control incoming calls. With the switch in the ON (auto-answer disable) position, the DMR11 asserts DTR immediately following system initialization or Master Clear, allowing the DMR11 to answer an incoming call. The call, however, is not terminated until the user program issues a Halt Request or the remote end terminates the call.

NOTE

1. **The ON to OFF transition of RI starts the DMR11 20 second timer. For the auto-answer feature to be affective, the "Ring Indicator Constantly ON after Call" option on the modem must not be installed.**

2. **Asserting DTR after Master Clear is required to maintain compatibility with DMC11.**

When the auto-answer feature is enabled, and when RI is detected, the DMR11 takes the appropriate action as described below:

1. Before Base In/Control In (Remote Load Detect Enabled)

   Remote load detect is enabled when the bootstrap password is not 377. When the DMR11 detects the ON to OFF transition of RI, it starts a 20 second timer. If a valid Enter MOP message is not recieved before the timer expires, the DMR11 drops DTR and waits up to two seconds for DSR to clear before asserting DTR again for the next call. The number of call set up failures are counted in the CFAIL error counter.

NOTE

If RI is not asserted by the modem on an incoming call and the modem sets DSR, the DMR11 starts the 20 second call set up timer.

2. Before Base In/Control In (Remote Load Detect Disabled)

   Remote load detect is disabled when the bootstrap password is 377. When the DMR11 detects RI, it drops DTR to disconnect the incoming call.

3. After Base In/Control In

   When the DMR11 detects RI, it asserts DTR and starts a 20 second timer. If the DMR11 does not receive a valid DDCMP header and DSR before the timer expires, it drops DTR and waits up to two seconds for DSR to clear before asserting DTR again for the next call. The number of call set up failures are counted in the CFAIL error counter.

3.7.2.2 Data Set Ready Glitch – In ISTRT, ASTRT, Run, or Maintenance Mode, once the DMR11 has received data set ready (Circuit CC/107), any DSR drop is reported by the DMR11 to the user program via a Control Out/Disconnect Error. It is not a fatal error. When the DMR11 drops DTR on a call set up time out, the DSR drop is not reported by Control Out.

3.7.2.3 RTS - CTS Delay – Any time the DMR11 attempts to transmit by presenting RTS (Circuit CC/105) to the modem, it will wait up to two seconds for CTS (Circuit CB/106) to be returned. If the two second time out occurs, the DMR11 will increment a CTS Fail Counter in its memory. If DMR11 is not in the Halt state, this counter will be updated to the Base Table in PDP-11 and VAX-11/780 memory.

NOTE

DMR11 exits from the HALT state after the user program has issued Base In and Control In.

3.7.2.4 Loss of Carrier Detect – Whenever Carrier Detect (Circuit CF/109) is dropped by the modem for greater than 500 ms while the DMR11 is still receiving, the carrier detect lost counter in DMR11 memory will be incremented. If DMR11 is not in the Halt state, then the error counter in the Base Table will also be updated.

3.7.2.5 Receiver Inactive Check – In ISTRT, ASTRT, Run, or Maintenance states, the following receiver inactive checks are made:

- In full-duplex mode, if a valid message header, including SOH, ENQ or DLE, has not been received in 20 seconds, a receiver inactive counter is incremented.

- In half-duplex mode, if the total selection interval time, before a valid DDCMP header is received, is about 20 seconds, the receiver inactive counter is incremented.

3.7.2.6 Modem Status Read During Input Command – This feature provides the user program with the option of reading (monitoring) modem status. Modem status is updated by the DMR11 to SEL 4 and BSEL 6 each time RDI is asserted in response to RQI. Refer to section 3.2.3.2 for details on this feature.

3.7.2.7 Data Terminal Ready Control – The DMR11 microcode controls the data terminal ready signal as follows:

1. DTR is set when:
   a. Master clear is performed,
   b. Auto-Answer (E134 switch 9 OFF) is enabled and the DMR11 detects RI, or
   c. The user issues Control In.
2. DTR is cleared when:
   a. The system powers down,
   b. The user issues Halt Request, or
   c. The 20 second call set up timer expires.

NOTE
If the link is established (DSR asserted) and auto-answer is enabled, the DMR11 drops DTR 20 seconds after a Master Clear (provided that Base In/Control In are not issued).

3.8 DMR11 DATA LINK FUNCTIONS

The DMR11 implements DDCMP and provides a number of functions to the user during what is referred to as a session. A session is defined as that period beginning immediately after the user assigns Base In and Control In and ending when the user issues a Halt Request or a fatal error occurs, forcing the DMR11 to shut down.

The functions that are provided during each of these sessions are listed below:

1. Creates an error-free data path. DMR11 transfers data between protocol users over a physical link, while maintaining data integrity within some small undetected error probability.
2. Transfers messages in proper sequence. Messages will be delivered from one user to the other in the same order as they are sent, even though the DMR11 may require the use of retransmission for error recovery.
3. Manages the characteristics of the channel. If the channel requires arbitration of transmission requests, the DMR11 is responsible for that management.
4. Interfaces to modem control signals. The DMR11 interfaces with signals necessary for the operation of the physical channel.
5. Accesses data in blocks consisting of byte quantities. The DMR11 accepts data in blocks consisting of 8-bit bytes. All 256 8-bit combinations are transmittable and transparent to DDCMP. However, the CRC-16 error detection polynomial used is most effective with blocks up to 4093 bytes long.

6. Provides restart or initialization notification. If the other end of the link resets or initializes, the DMR11 will notify the user.

7. Provides start and stop control. The user controls the protocol and can start (or reinitialize), and stop (or halt) the operation of the DMR11.

8. Provides notification of channel error. When a persistent error is detected, the user is notified of such a condition. Such errors might be (a) a high bit error rate; (b) outages; (c) nonexistent communications; or (d) modem failure.

9. Provides a maintenance mode. The DMR11 creates a data envelope with bit error-detection-only capability for use in diagnostic testing and system bootstrapping functions.

NOTE

In order to recover from the premature termination of a session, forcing DMR11 to shut down, by a hardware or modem failure, the user should implement higher level protocols to ensure synchronization of the two communicating devices between sessions. Since the DMR11 or DDCMP guarantees these functions within each session only, it is the user's responsibility to implement a higher level protocol in order to provide an additional level of error recovery, guaranteed delivery, and sequentiality.

CHAPTER 4
SERVICE

4.1 SCOPE

This chapter provides information for servicing the DMR11. It includes the maintenance philosophy, maintenance functions, preventive maintenance, and corrective maintenance. The section on corrective maintenance contains brief descriptions of the diagnostics associated with the DMR11.

4.2 MAINTENANCE PHILOSOPHY

The field replaceable unit (FRU) for the DMR11 is either a faulty module or cable. Training of field service personnel is directed to functional and application troubleshooting, using diagnostics, for fault isolation to the FRU. Spare parts for module repair are not stocked in the field. Typical applications of the DMR11 do not permit lengthy troubleshooting sessions and component troubleshooting/repair requires, at least, a 16-channel logic analyzer.

CAUTION

When inserting or removing the M8207-RA microprocessor module, be sure not to dislodge the priority plug or control read only memories (CROMs).

Ensure that the CROM is seated firmly and in the proper socket; otherwise erratic operation of the DMR11 may result.

4.3 MAINTENANCE FUNCTIONS/MAINTENANCE MODES

The maintenance functions are available to the DMR11 via the maintenance control and status register (CSR) (BSEL 1). Maintenance and system tests constitute the Maintenance Modes.

4.3.1 Maintenance Register (BSEL 1)

This register contains the high byte of address 76XXX0. A brief description of the CSR byte is provided in Chapter 3. The byte format and bit descriptions are provided in detail in this section.

15	14	13	12	11	10	9	8	
RUN	MCLR	MICRO DIAG	STEP LU	LU LOOP	ROM OUT	ROM IN	STEP UP	BSEL 1

BSEL 1 contains all maintenance functions, including Master Clear, and is not intended for normal user communications between the PDP-11 program and the microprocessor. These functions override all other control functions. All bits are read/write; only Master Clear is functional if the BSEL 1 Lock Out switch is set (refer to Chapter 2). Table 4-1 describes the bit functions of BSEL 1.

4.3.2 Maintenance Modes

The DMR11 microprocessor can be tested by two basic modes:

- Maintenance and
- System Test (free-running).

The DMR11 line unit can be tested by three basic modes:

- Single Step Internal Maintenance,
- System Test Internal Maintenance, and
- External Maintenance.

4.3.2.1 Maintenance Mode – The Maintenance Mode can be invoked using selected bits of BSEL 1. These can be used to halt the microprocessor (clear bit 15), step the microprocessor (set bit 8), examine the current CROM location (assert bit 10 and examine SEL 6), and override the current CROM instruction with a different instruction and execute the new instruction (load SEL 6 with the new instruction, assert bits 8 and 9, then clear bit 8).

NOTE

1. **Be sure that BSEL 1 Lock Out BST Switch 1, E85 is ON to allow access to the maintenance bits in BSEL 1.**

2. **With the BST switch OFF, it is still possible to Master Clear the microprocessor by setting bit 14 of BSEL 1.**

4.3.2.2 System Test – System Test Mode tests the functionality of the microprocessor and line unit running at full speed and utilizing the control ROM.

NOTE

Run Inhibit Switch 7, E28 must be ON to use this mode and ensure normal operating conditions.

4.3.2.3 Single Step Internal Maintenance Mode – This mode is selected by the user program setting LU Loop and clearing Run bits 11 and 15 of SEL 0. This mode allows for checking most of the line unit without disconnecting the M8203 from the modem or from the triaxial cable. Line unit signal D8 LPBKL is set to keep the transmitter output active, looping the output back at TTL levels to become the receiver input. Line unit Request to Send (RTS) and Data Terminal Ready (DTR) signals are held cleared. The clocking source is the D16 Step LU signal from the microprocessor which becomes D1 Step LU at the line unit. The user program generates the clock signal which sets Step Line Unit bit 12 of SEL 0.

4.3.2.4 System Test Internal Maintenance Mode – This mode is selected by the user program setting Line Unit Loop bit 11 and bit 15 (Run) of BSEL 1. This mode allows the program to perform an off-line system test by free-running the DMR11 and checking the line unit without disconnecting the M8203 from the modem or from the triaxial cable. The transmitter output is looped back at TTL level to become the receiver input. The clock source is the DMR11 maintenance clock which is 48K b/s.

4.3.2.5 External Maintenance Mode – External Maintenance Mode is selected by the user program placing the DMR11 in normal running mode (bit 11 clear and bit 15 set) and terminating the cables with a test connector.

The M8203 options are configured as follows:

1. **DMR11-AA (for RS-232-C; RS-423-A)**

   - The modem must be disconnected and the H325 test connector must be attached to the BC05D-25 cable.

   - Data rate switches (switches 8, 9, and 10 of E39) select the clock rate. This clock signal is looped back in the H325 to simulate modem transmit and receive clocks. The data rate for this application must not exceed 56K b/s.

   - Modem control signals are tested for proper level conversion and cable paths. These signals are looped back in the H325 as shown in the signal flow of Figure 2-5E.

2. DMR11-AB (CCITT V.35/DDS)

   - The modem must be disconnected and the H3250 test connector must be attached to the BC05Z-25 cable.

   - Data rate switches (8, 9, and 10 of E39) select the clock rate. This clock signal is looped back in H3250 to simulate modem transmit and receive clocks.

   - Modem control signals are tested for proper level conversion and cable paths. These signals are looped in the H3250 as shown in the signal flow of Figure 2-5B.

3. DMR11-AC (for Integral Modem local use)

   - The local link connections of the BC55A connector panel are disconnected at the local panel and the FDX switch on the BC55A connector panel is switched to half-duplex to accomplish the external loopback.

   CAUTION
   If DMR11 is connected to another running DMR11, disconnect the cable at the BC55A connector panel during diagnostic execution.

   - Data rate switches (8, 9, and 10 of E39) select the clock rate. This data is looped back through the BC55A connector panel to test, transmit, and receive data. The data rate for this application must not be less than 50K b/s.

4. **DMR11-AE (for RS-422-A interface)**

   - The modem is disconnected and a H3251 test connector is attached to the BC55D-33 cable.

   - Data rate switches (8, 9, and 10 of E39) select the clock rate. This signal is looped back through the H3251 to simulate modem transmit and receive clocks.

   - Modem control signals are tested for proper level conversion and cable paths. These signals are looped in the H3251 as shown in the signal flow of Figure 2-5D.

4.3.3 Maintenance (LED) Indicators

Six light emitting diodes (LEDs) are installed on the M8203 line unit to permit visual observation of certain conditions. Five of these pertain specifically to modem conditions. The remaining LED (D15) reflects operational conditions of the DMR11. Table 4-2 provides a description of each LED, while Figure 4-1 identifies the physical locations.

Table 4-1 BSEL 1 Bit Descriptions

Bit	Name	Description
8	Step μP (Step Microprocessor)	When set, it steps the microprocessor through one instruction cycle which is typically composed of three, 60 ns pulses. The Run bit should be cleared before executing this control function.
9	ROM In	When set, it directs the contents of BSEL 6 and 7 as the next microinstruction to be executed by the microprocessor when Step μP is set.
10	ROM Out	When set, it modifies the source paths for BSEL 6 and 7 to contain the contents of the addressed CROM. If ROM Out and Step μP are set, then the content of the next CROM address will be output to BSEL 6 and 7.
11	LU Loop (Line Unit Loop)	When set, it connects the line unit's serial line OUT, back to its serial line IN. This loop back is done at the TTL level before level conversion. When the LU Loop bit is set and the Run bit (bit 15) is cleared, the Step LU clock is the only one available for shifting data in or out. When the LU Loop bit is set and the Run bit is set, data is clocked at 48K b/s by the maintenance clock. If the LU Loop bit is cleared and the Run bit set, the loop back test connector is required.

LU loop	Run	Clock Source	Mode
Set	Clear	Step LU(bit 12 via Pro gram	Single -Step Internal Mainten-ance
Set	Set	Maintenance Clock @ 48K b/s	System Test Internal Mainten-ance
Clear	Set	Maintenance Clock determined by rate select SWs	External Mainten-ance

Table 4-1 BSEL 1 Bit Descriptions (Cont)

Bit	Name	Description
	NOTE **The DMR11 must be set up in full-duplex mode to run in any loopback maintenance mode. For External Loopback Mode, cable test connectors H325, H3250 or H3251, or module test connectors H3254 or H3255 are required.**	
12	Step LU (Step Line Receiver)	With the Run bit cleared and bit 12 set, the transmitter shifts; when bit 12 is cleared, the receiver shifts. This control function is used in conjunction with LU Loop bit 11 to simulate transmit and receive clocks for line unit maintenance in Single Step Maintenance Mode.
13	MICRO DIAG (Micro Diagnostics)	This bit, in addition to the position of Switch 10 on Switch Pack E134, enables automatic execution of internal microdiagnostics. Refer to Table 2-11 for further conditioning information.
14	MCLR (Master Clear)	When bit 14 is set, MCLR initializes both the microprocessor and the line unit. This bit is self clearing. The microprocessor clock is enabled and the Run bit is set, placing the DMR11 in the initialized state.
15	Run	Run controls the microprocessor clock; bit 15 is set by BUS initialization or Master Clear, which enables the microprocessor clock. Run can be cleared for maintenance by the Run Inhibit switch (E28). See D16 of the *M8207-RA Print Set*. The BST switch is provided to prevent Run from being cleared by a runaway microcode program when the microprocessor malfunctions. Further discussion of the Run Inhibit switch is contained in Chapter 2.

4.4 PREVENTIVE MAINTENANCE (PM)

There is no specific DMR11 PM schedule. A general check of voltages and connections should be done when system PM is performed. After handling DMR11 modules or cables, a complete checkout of the device, by running all diagnostics and, if possible, the interprocessor test, is required. Special care must be exercised for the following reasons:

- The DMR11 is susceptible to seating problems and
- CROM (control ROM) chips installed in sockets are easily dislodged during removal and replacement of the M8207-RA module or adjacent modules. The CROM chips may accidentally come in contact with the etch side of the adjacent module.

4.5 CORRECTIVE MAINTENANCE ON A PDP-11 PROCESSOR

Since the FRU is either a module or cable, all corrective diagnosis should be directed towards isolating the failing FRU. DMR11 diagnostics are designed to aid in the isolation process and should be run

Table 4-2 Maintenance Indicators

Designation	Name	Description
D10	Signal Quality	A signal from the modem that indicates the presence or absence of the carrier. Usually, when this signal is ON it indicates the presence of the carrier and OFF indicates an absence of the carrier.
D11	Carrier	Indicates that the carrier is present at the receiver.
D12	Receiver Data	When ON, indicates that a steady stream of 1s are being received.
D13	Transmit Data	When ON, indicates that a steady stream of 1s are being transmitted.
D14	Request to Send	When ON, indicates that the USYRT is ready to start transmitting as soon as Clear to Send is detected.
D15	Heartbeat	At Master Clear time, this indicator is OFF. When the DMR11 asserts the Run bit, this indicator will go ON and remain ON until the completion of Base In and Control In. Following Control In, this indicator will blink at the rate of five times per second until a Halt or fatal error condition occurs, at which time it will remain ON. This sequence is graphically represented in Figure 4-1.

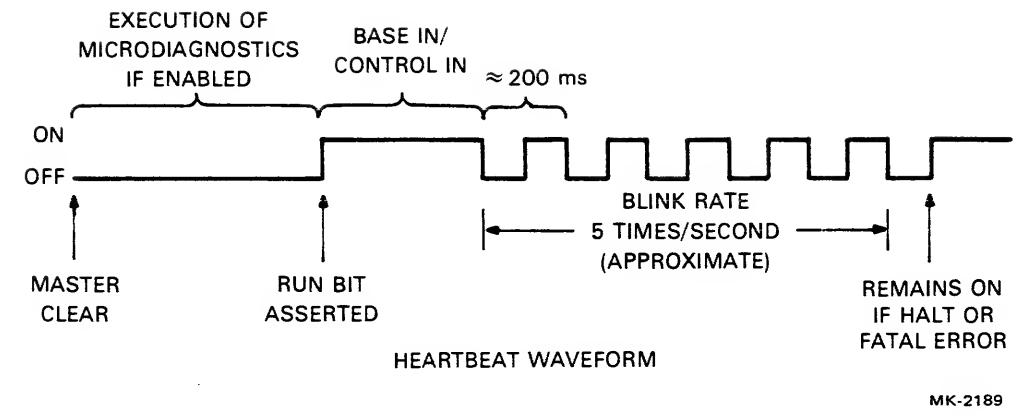
starting with the basic microprocessor test and continuing to the interprocessor test. The proper sequence of diagnostics is as follows:

Diagnostic	Description
CZDMP*	M8207 Static Diagnostic 1
CZDMQ*	M8207 Static Diagnostic 2
CZDMR*	M8203 Static Diagnostic 1
CZDMS*	M8203 Static Diagnostic 2
CZDMI*	DMR11 Functional Diagnostic
ZITAD*/ZDMO**	DMC11 11/DMR11 ITEP-OVERLAY Interprocessor Test

4.5.1 CZDMP*/CZDMQ*

These diagnostics test the M8207-RA microprocessor in two parts and by using the diagnostic supervisor (DS). Through dialogue with the operator, the program allows modification of device parameters, such as the UNIBUS address, vector address, and processor type.

*Indicates current revision level of diagnostics.



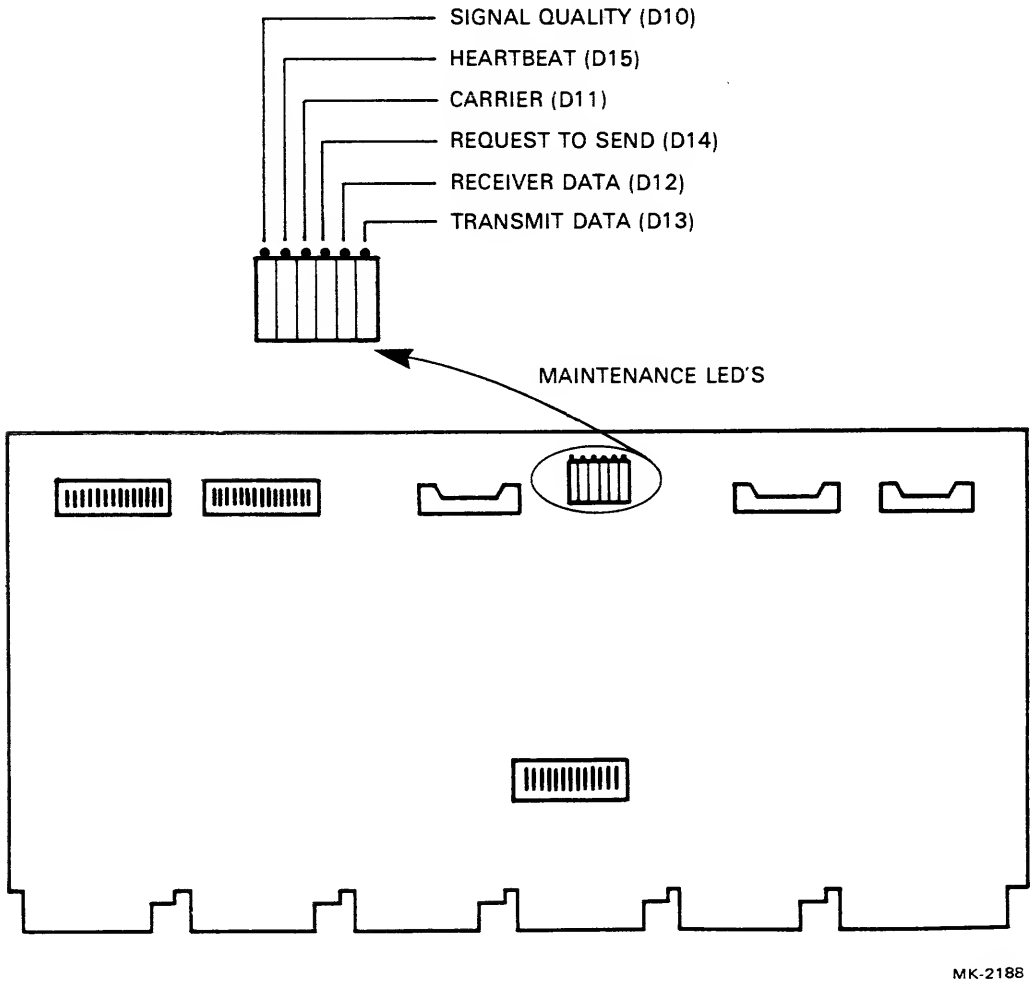


Figure 4-1 M8203 Maintenance LED Locations/Heartbeat Waveform

This program is compatible with the stand-alone diagnostic supervisor. It must be loaded co-resident with the DS, or be previously combined with the DS and loaded as a single file. In either case, the combined program will not exceed 16K of memory. Refer to Appendix C for details on the diagnostic supervisor.

The total time required to run M8207 static tests is approximately from 30 seconds to 2 minutes per pass, depending on the CPU type.

CZDMP* and CZDMQ* are compatible with XXDP+, ACT/SLIDE, and APT. XXDP+ and ACT/SLIDE may be run in dump or chain modes. APT can be run in program or script modes.

Memory management is not used in this program and, if installed, it is disabled. If parity memory is installed, memory parity traps are disabled.

An error log retains the number of errors which have occurred on each device under test since the last start or restart command. The log may be printed by using the print command.

A summary of the tests performed are listed in Tables 4-3 and 4-4. All tests support the DMC11, KMC11-A, B, and DMR11. However, some tests listed in Table 4-4 are not executed on certain devices. Refer to Table 4-4 for these exceptions. For greater detail, refer to the diagnostic listings.

Table 4-3 CZDMP* Diagnostic Summary

Test Number	Description
1	Verify that referencing UNIBUS device registers does not cause a T/O trap.
2	Verify that Run can be cleared.
3	UNIBUS register word, dual addressing test
4-8	Control status register write/read tests
9	Port 4 register write/read test
10	Port 6 register write/read test
11	UNIBUS register byte, dual addressing test
12	Maintenance instruction register test
13	Microprocessor test
14-27	Microprocessor IBUS/IBUS* register write/read tests
28	Microprocessor IBUS/IBUS* dual address test
29	Microprocessor BR register test
30	Scratchpad test
31	Scratchpad dual addressing test
32,33	Interrupt tests
34,35	Priority interrupt tests
36-38	NPR tests
39,40	Test of extended address (EA) bits 16 and 17
41,42	NPR non-existent memory test
43	NPR test
44	ALU C-bit test
45-76	ALU tests

4.5.2 CZDMR*/CZDMS*

These diagnostics perform static tests of all M8203 logic. These include – line unit register addressing, USYRT addressing, static bit interaction and read/write logic tests, basic transmitter, receiver sequencing and data buffering, and static operations in character and bit-stuffing modes. In addition, data messages are sent on the line unit at TTL level, or through an external test connector with a specific modem interface selected.

Static logic tests provide troubleshooting capabilities such as tight scope loops, switch options, and the ability to lock on intermittent errors. Additional tests provide fault isolation to facilitate replacement of the smallest field replaceable unit.

Table 4-4 DZDMQ* Diagnostic Summary

Test Number	DMC 11	KMC11-A	KMC11 -B	DMR 11	Description
1					Verify that referencing UNIBUS device registers does not cause a timeout.
2					BR right shift test
3,4	S				IOP CRAM write/read test
5	S				IOP CRAM dual addressing test
6,7					IOP main memory test
8					IOP main memory dual addressing test
9	S	S			IOP MAR test (4K Main Memory)
10	S				IOP (CRAM) ODT bits test
11	S		S	S	CRAM tests of Jump(i)
12-24	S				CRAM tests of Jump(i)
25	S	S			4K Main memory page dual address test
26	S	S			Jump Field, page test
27,28	S	S			Jump test
29	S	S			Z bit test
30	S	S			C bit test
31					Program clock bit test
32					Force Power Fail test
33					Microprocessor noise test
34					NODST instruction test
35	S	S		S	Extended CRAM test (M8206 only)
36	S	S		S	Microcode test (M8206 only)
37					Negative address test
38					Byte addressing test
39	S	S	S		PC register test
40	S	S	S		Branch Field H test
41					Scratchpad 0 (SP0) selection test
42	S	S	S		MOV INST H signal test
43					Master Clear test

S = Test Skipped

These programs conform to the stand-alone version of the diagnostic supervisor and are compatible with ACT, APT, XXDP+, and SLIDE.

Through dialogue with the operator, the programs permit modifications of device parameters such as the UNIBUS address, vector addresses, and device priority. The operator can specify particular tests to be run and a variety of looping, running, and reporting modes. Refer to Appendix C for details on the diagnostic supervisor.

Device errors are reported as they occur. The report includes the test number and error description, good and bad test data, and applicable device register contents.

A summary of the tests performed are listed in Tables 4-5 and 4-6. For greater detail, refer to the diagnostic listings.

4.5.3 CZDMI*

The CZDMI* diagnostic performs testing on the DMR11 option in a functional manner to verify its proper operation under microcode controlled use of the DDCMP. This includes a ROM CRC/CCITT check, microdiagnostis, command utilization, error generation, interrupt testing, and interrupt driven exercising.

Table 4-5 CZDMR* Diagnostic Summary

Test Number	Description
1	Microprocessor CSR addressing test (SEL 0)
2	Inbus/Outbus register 14 initialization test
3	Inbus/Outbus register 14 read/write bit test
4	Register 14 Master Clear test
5	Register 14 UNIBUS reset (INIT) test
6	Line unit false selection test
7	Inbus register Master Clear test
8	Register 10-17 addressing test
9	Register 11 read/write bit test
10	Register 12 read/write bit test
11	Register 13 read/write bit test
12	Register 17 read/write bit test
13	Maintenance clock bit test
14	Extended register Master Clear test
15	Extended register addressing test
16	Registers 15, 16/AX2-15, AX2-16 read/write bit test
17	AX0-15, AX0-16 read/write bit test
18	AX1-15, AX1-16 read/write bit test
19	AX3-15, AX3-16 read/write bit test
20	Register 17 AX2-16 read/write, Master Clear test
21	Transmitter buffer data test
22	Transmitter buffer sequencing test
23	TX MSG timing test, character mode with CRC
24	TX MSG timing test, bit mode with CRC
25	TX MSG timing test, character mode with no CRC
26	TX UNDERRUN set and clear test, character mode
27	TX character length timing test, character mode with CRC
28	TX character length timing test, bit mode with CRC
29	TXDATA bit test, character mode with no CRC
30	USYRT RCV MSG test, character mode with CRC
31	USYRT RCV MSG test, bit mode with CRC
32	USYRT RCV MSG test, character mode with no CRC
33	USYRT RCV MSG test, bit mode with no CRC
34	Silo-disabled transmitter load test
35	Silo-disabled MSG test, bit mode with no CRC
36	RCV buffer test, character mode with CRC
37	RCV character length timing test, character mode with no CRC
38	RCV character length timing test, bit mode with no CRC
39	TX UNDERRUN error, idle marking character mode with no CRC
40	MSG termination with Go Ahead (GA) characters, bit mode with no CRC
41	Idle SYNC test, character mode
42	STRIP SYNC test

This functional test provides troubleshooting capabilities such as tight scope loops, switch options, and the ability to lock on intermittant errors. Additionally this program conforms to the standalone version of the diagnostic supervisor and is compatible with APT, ACT, XXDPT, and SLIDE. Refer to Appendix C for details on the diagnostic supervisor.

Table 4-6 CZDMS* Diagnostic Summary

Test Number	Description
1	Bit stuffing test
2	RCV OVERRUN error, set and clear test
3	Abort sequence test
4	Abort and idle flags test
5	TX underrun error, idle abort characters, bit mode
6	RCV disable test
7	Assembled bit count test
8	Secondary station address bit test
9	All parties address bit (RDALL) test
10	Insert error bit (IERR) test, character mode with no CRC
11	Switch PACK printout and test
12	Register AX3-15 printout
13	CRC generation test
14	CRC error detection test
15	VRC parity generation test
16	VRC error detection test
17	Integral modem interface test, character mode with CRC
18	V.35 modem interface test, character mode with CRC
19	RS-232-C and RS-423-A modem interface test, character mode with CRC
20	RS-422-A modem interface test, character mode with CRC
21	Half-duplex bit (HALF DUPX) test
22	Half-duplex RCV disabled test, with silos disabled
23	Interaction of modem control bits
24	Data test, bit mode with no error detection
25	Data test, character mode with no error detection
26	Data test, bit mode with CRC-CCITT-1 error detection
27	Data test, bit mode with CRC-CCITT-0 error detection
28	Data test, character mode with CRC-16 error detection
29	Data test, character mode with ODD VRC error detection
30	Data test, character mode with EVEN VRC error detection
31	Contiguous ones in secondary station address mode, bit mode
32	DDCMP MSG test, character mode

Through dialogue with the operator, the program permits modification of device parameters such as the UNIBUS address, vector addresses, and device priority. The operator can specify particular tests to be run and a variety of looping, running, and reporting modes.

A summary of the tests performed are listed in Table 4-7. For greater detail, refer to the diagnostics listings.

4.5.4 DMR11 Microdiagnostic Error Reporting

When the microdiagnostic is run on the DMR11 (during power-up/initialize), status indications take the following form (see table below):

1. Upon completion of the microdiagnostic, if BSEL 1 has the Run bit set and BSEL 3 contains 200_8, then the test has run to completion successfully and the DMR11 is considered healthy.

2. After attempting the microdiagnostic, if BSEL 1 has the Run bit set and BSEL 3 equals 100_8, then the microdiagnostic tests were inhibited.

3. A failure in the microprocessor module is indicated by no Run bit in BSEL 1 and a 001_8 (or any other indication other than 200_8, 100_8, or 002_8) in BSEL 3 after initiation of the microdiagnostic.

4. The line unit is the suspect module when no Run bit is set in BSEL 1 and a 002_8 is present in BSEL 3 after the microdiagnostic.

BSEL 1	BSEL 3	Indication
Run bit	200_8	Test complete
Run bit	100_8	Test inhibited
no Run bit	001_8 or XXX	M8207 test failed
no Run bit	002_8	M8203 test failed

Table 4-7 CZDMI* Diagnostic Summary

Test Number	Description
1	Verify all CSR addresses
2	ROM CRC/CCITT check
3	Master Clear/Microdiagnostics
4	Initialize/Base In
5	DMR Commands
6	Control In commands
7	Modem test
8	No Buffer test
9	NXM (Base In, BA/CC IN RCV & XMT)
10	Time Out
11	MSG Too Long
12	Procedure Errors
13	Free Running Flag Mode
14	Extended Addressing
15-16	Interrupt/Base In Resume (124 bytes to 2K bytes depending on memory availability)
17	Interrupt Driven Exercise (64 Buffers – 16 bytes to 256 bytes depending on memory availability)
18	Interrupt Large Message (2K bytes to 16K bytes depending on memory availability)
19	Interrupt Maintenance Mode (2K bytes to 16K bytes depending on memory availability)

4.5.5 ZDMO** – DMC11/ DMR11 Overlay for Interprocessor Test Program (ITEP)

This test is used to isolate various interconnect problems between systems. Through a series of tests, failures are identified in level converters, cables and connections, modems, lines between modems, and modem incompatibilities.

ITEP has been useful in identifying new or modified software problems. In this role, ITEP is used to isolate the hardware from the system software. Typically, if ITEP runs, the system software should run. ITEP provides a controlled environment for test purposes often unavailable in operating systems.

ITEP can be used for loop testing, providing the ability to incrementally test larger (or smaller) segments of the communications link. For instance, if a failure occurs when running in Modem Analog Loop Mode rather than in Cable Loop Mode (with an H325 connector), the probability of a modem or modem option fault is increased.

ITEP is more of a confidence test than a true diagnostic, and provides a GO/NO-GO indication of the integrity of the communications link. ITEP is often used for installation acceptance, as well as confirmation of a corrective action.

An ITEP feature not provided in any of the stand-alone diagnostics is the capability of checking out the remote load detect (RLD). The DMC11/DMR11 overlay for the Interprocessor Test program is designed to verify the proper operation of a complete communications link (DMC11 or DMR11) from one PDP-11 system to another, or to a communications test center. The program must be used in conjunction with the Interprocessor Test Monitor program (ZITAD*) on a PDP-11 system. Two tests for the DMR11 are selectable by the parameter locations provided in ITEP. To aid in Link Test analysis, refer to Table 4-8.

TEST 1 is a link test which provides a GO/NO-GO test (a confidence check) on the communications link (could be either half-duplex or full-duplex).

TEST 2 is a bootstrap test which checks the ability of a DMR11 to boot another DMR11 using maintenance operation protocol (MOP) messages. The bootstrap test requires an M9301-YJ/M9312 (UNIBUS terminator with bootstrap) or equivalent boot module at one station.

The RLD feature of the DMR11 is checked out: the host sends an Enter MOP message to a remote station to initialize the entire system and cause program control to be transferred to a boot ROM program (or in true on-line application, a secondary boot program) to be down-line loaded and eventually execute that program.

Only the down-line load feature of the DMR11 can be checked: a remote station sends a program Request MOP Message and the host, with its DMR11 running ITEP, will down-line load a special program to the remote station, which prints out a message indicating a successful BOOT has been completed.

NOTE

1. **Refer to Appendix E for detailed operating procedures for bootstrap testing under the ITEP program.**

2. **Refer to the diagnostic listings for detailed operating procedures of CZDMP*, CZDMQ*, CZDMR*, CZDMS*, and CZDMI*.**

4.5.6 DEC/X11 DMC11 Module

The DEC/X11 DMC11 module, DMC*, is designed to exercise up to and including two consecutively addressed DMR11 synchronous interfaces. One pass of the DMC* module consists of transmitting and receiving seven buffers of 100 characters, 100 times for each selected device.

It is recommended that bit 0 of the DMC* Switch Register 1 (SR1) be set to 1 and that a test connector be installed (H325, H3250, or H3251 for M8203) when running DEC/X11 (as indicated in the checkout procedures in Chapter 2).

Installing the test connector and setting bit 0 of SR1 allows the DMC11/DMR11 to run in External Loopback Mode and, therefore, generate more activity on the UNIBUS.

Table 4-8 DDCMP Message Decode for DMR11**

Type of Message	Code	Class	Count Bits 7-0	Flag 2 Bits S Q	Count Bit 13-8	Response	Sequence	Address Point To Point
Start Message	Bits	00000101	00000110	1 1	000000	00000000	00000000	00000001
	Hex	0 5	0 6		C 0	0 0	0 0	0 1
	ASC11	ENQ	ACK		@	NUL	NUL	SOH
Start Acknowledgement	Bits	00000101	00000111		000000	00000000	00000000	00000001
	Hex	0 5	0 7		C 0	0 0	0 0	0 1
	ASC11	ENQ	BEL		@	NUL	NUL	SOH
Acknowledgement	Bits	00000101	00000001	S Q	000000	No. Last Good Msg. Rcvd.	00000000	00000001
	Hex	0 5	0 1		* C 0	"	0 0	0 1
	ASC11	ENQ	SOH		* @	"	NUL	SOH
Data Message	Bits	10000001	No. of Char.	S Q	No. of Char.	"	No. Msg. Sent	00000001
	Hex	8 1	"	S Q	"	"	"	0 1
	ASC11	SOH	"	S Q	"	"	"	SOH
Negative Acknowledgement BCC Header Error	Bits	00000101	00000010	S Q	000001	"	00000000	00000001
	Hex	0 5	0 2		* C 1	"	0 0	0 1
	ASC11	ENQ	STX		* A	"	NUL	SOH
Negative Acknowledgement BCC Data Error	Bits	00000101	00000010	S Q	000010	"	00000000	00000001
	Hex	0 5	0 2		* C 2	"	0 0	0 1
	ASC11	ENQ	STX		* B	"	NUL	SOH
Negative Acknowledgement Buffer Unavailable	Bits	00000101	00000010	S Q	001000	"	00000000	00000001
	Hex	0 5	0 2		* C 8	"	0 0	0 1
	ASC11	ENQ	STX		* H	"	NUL	SOH
Negative Acknowledgement Receiver Overrun	Bits	00000101	00000010	S Q	001001	"	00000000	00000001
	Hex	0 5	0 2		* C 9	"	0 0	0 1
	ASC11	ENQ	STX		* I	"	NUL	SOH
Negative Acknowledgement Message Too Long	Bits	00000101	00000010	S Q	010000	"	00000000	00000001
	Hex	0 5	0 2		* D 0	"	0 0	0 1
	ASC11	ENQ	STX		* P	"	NUL	SOH
Negative Acknowledgement Header Format Error	Bits	00000101	00000011	S Q	010001	"	00000000	00000001
	Hex	0 5	0 2		* D 1	"	0 0	0 1
	ASC11	ENQ	STX		* Q	"	NUL	SOH

*Assumes that both S and Q are asserted

Table 4-8 DDCMP Message Decode for DMR11** (Cont)

Type of Message	Code	Class	Count Bits 7-0	Flag 2 Bits S Q	Count Bit 13-8	Response	Sequence	Address Point to Point
Reply Message	Bits	00000101	00000011	S Q	00000000	00000000	No. Last Msg. Sent	00000001
	Hex	0 5	0 3	*	C 0	0 0	"	0 1
	ASCII	ENQ	ETX		@	NUL	"	SOH
Negative Acknowledgement Reply Response	Bits	00000101	00000010	S Q	000011	No. Last Good Msg. Rcvd	00000000	00000001
	Hex	0 5	0 2	*	C 3	"	0 0	0 1
	ASCII	ENQ	STX		C	"	NUL	SOH
Maintenance Message	Bits	10010000	No. of Char.	1 1	No. of Char.	00000000	00000000	00000001
	Hex	9 0	"		"	0 0	0 0	0 1
	ASCII	DLE	"		"	NUL	NUL	SOH

* Assumes that both S and Q are asserted

External loopback connector options are:

DMR11-AA	-	H325 or H3251
DMR11-AB	-	H3250
DMR11-AC	-	HDX switch selected on the BC55A panel implements turnaround
DMR11-AE	-	H3251

Speed is selected by switches 8, 9, and 10 on E39, (refer to Table 2-9).

4.5.7 Soft Error Reports Under DEC/X11

Soft errors indicate errors which occurred causing a message retransmission. A cumulative count of soft errors is kept in DMR11 random access memory (RAM) memory. The RAM memory is written to PDP-11 memory (beginning at the assigned base address) whenever a fatal DMR11 error occurs at the end of each pass.

DEC/X11 checks the error counters in the Base Table at the end of each pass. If any errors are counted, they are reported as soft errors.

The soft error report may be used in the isolation of certain DMR11 failures from UNIBUS loading or data late problems.

The DMR has no data late bit or capabilities for detecting the fact that it did not obtain Bus mastership in time to service the synchronous line. The DMR11 sees such a condition as an error in the synchronous data stream (a BCC error transmitter underrun or receiver overrun) and DDCMP causes the message to be retransmitted. This occurrence causes incrementation of the cumulative error counters in DMR11 RAM memory.

A process of elimination must be used to determine whether soft errors (BCC) are caused by BUS latency or failing DMR11 hardware.

Typically, the DMR11 should show no errors when running in a local loopback mode. This is normally a noise-free circuit. Therefore, any soft error reports should be examined and the cause isolated.

If soft errors are reported while running a DMR11 on a fully loaded system (other devices being exercised simultaneously), they may be due to Bus latency. This may be verified by running only the DMC* DEC/X11 module with only one DMR11 enabled. If the soft errors cease, a latency condition is indicated.

If soft errors persist while running only the DMC* DEC/X11 module, the DMR11 device diagnostics should be run. The problem could be a faulty DMR11 or cable.

SR1 (bit 0) may be used in the isolation process. If bit 0 is set, DEC/X11 does not set line unit loopback but it uses an external turnaround. By running with bit 0 clear, a TTL loopback is performed, eliminating the possibility of the cable/turnaround connector being faulty.

With the M8203, bit 0 clear eliminates the level converters and the Integral Modem. The bit rate selected is 48K b/s using the maintenance clock.

4.5.8 Examination of DMR11 Internal Components

The following are some examples for examining DMR11 memory and scratchpad registers.

Example 1: Examine DMR11 Memory

Procedures		Comments
1.	Load 0_8 SEL 0	;To clear Run bit and stop the ;microprocessor
2.	Load $010XXX_8$ to SEL 6	;Microinstruction ;is loaded into SEL 0 where XXX is an ;eight bit memory address which is ;loaded into MAR
3.	Load 1400_8 to SEL 0	;Set ROM In and Step μP bits
4.	Load 055224_8 to SEL 6	;Load microinstruction to SEL6 to read ;memory content pointed to by MAR to ;SEL4. MAR is incremented.
5.	Load 1400_8 to SEL 0	;Set ROM In and Step μP bits
6.	Examine BSEL 4 low byte for memory content	;BSEL 4 contains content of memory ;location under examination.
7.	Go to Step 5 for examination of consecutive memory locations	; ; ; ;

Example 2: Examine DMR11 Scratchpad Registers

Procedures		Comments
1.	Load SEL 0 with 0_8	;To clear Run bit
2.	Load SEL 6 with $0606XX_8$	;SEL 6 is loaded with microinstruc- ;tions, where XX is 0-17, Scratchpad ;Register content of SP is loaded into ;the Branch Register.
3.	Load SEL 0 with 1400_8	;Set ROM In and Step μp bits the micro- ;processor.
4.	Load SEL 6 with 061224_8	;Load microinstruction, where content ;of SPX (from BR) is loaded into BSEL ;4.
5.	Load SEL 0 with 1400_8	;Set ROM In and Step μP bits.
6.	Examine BSEL4 for content of SPX	;BSEL 4 contains contents of scratchpad ;X.

Example 3: DMR11 Base Table Dump

Procedures		Comments
1.	Load 43_8 to BSEL 0	To perform an RQI for Base I type input.
2.	Examine BSEL 0 for bit 7 (RDYI) set.	To indicate the microprocessors release of the port.
3.	Load 1000_8 to SEL 4	Giving base address to microprocessor.
4.	Load 0 to SEL 6	Clearing high order address bits and Resume bit.
5.	Load 203_8 to BSEL 0	To relinquish port back to microprocessor.
6.	Load 42_8 to BSEL 0	To force a Halt Function with RQI.
7.	Examine BSEL 0 for bit 7 (RDI) set.	To indicate the microprocessors release of the port.
8.	Load 202_8 to BSEL 0	To relinquish port back to microprocessor.
9.	Examine 128 memory locations starting at 1000 to see Base Table	To see counters, buffers, and other Base Table data. (Refer to the DMR11 Base Table layout of Figure 4-2.)

NOTE

This procedure provides a Base Table dump from a DMR11 in the DDCMP Halt state. If the DMR11 is in the DDCMP Run state and a Base Table dump is desired, only perform steps 6 through 9.

4.6 CORRECTIVE MAINTENANCE ON A VAX-11/780

Since the FRU is either a module or cable, all corrective diagnosis should be directed to isolating the faulty FRU. DMR11 diagnostics are designed to aid in the isolation process and should be run starting with the basic microprocessor test. The proper diagnostics sequence is as follows.

Diagnostic	Description
EVDXA REV *.*	COMM Microprocessor Repair Level Diagnostics
EVDMA REV *.*	M8203 Repair Level Diagnostics
EVDCA REV *.*	VAX Synchronous Link Level 2 Diagnostics

4.6.1 EVDXA COMM Microprocessor Repair Level Diagnostics

This diagnostic performs tests on the M8207-RA microprocessor. It includes device initialization, register and RAM addressing, READ/WRITE testing, interrupt generation and priority, NPR operation and addressing, ALU functions and the microprocessor instruction set, and INBUS/INBUS* and OUTBUS/OUTBUS* testing. This program performs many of the tests in Maintenance Mode by stepping the microprocessor through various instruction sequences. This program will be run at VAX Level 3, which is a stand-alone repair level.

```
BASE
TABLE
ADDRESS                          BASE TABLE ALLOCATION


        ;NAME
        ;----
        ;
000000  UPINDX  ;! BASE TABLE UPDATE INDEX POINTER
000001  UPLMT   ;! BASE TABLE UDPATE LIMIT
000002  BASTBL  ;# BEGINNING OF BASE TABLE DATA          (ALWAYS = 000)

000003  NRNBF   ;@ NAKS RCVD - BUFFER TEMP UNAVAILABLE (REASON =  8.)
000004  NRHCE   ;@ NAKS RCVD - HEADER BCC ERROR         (REASON =  1.)
000005  NRDCE   ;@ NAKS RCVD - DATA BCC ERROR           (REASON =  2.)

                ; ** --- IN DDCMP MAINTENANCE MODE THESE
                ;         IN-BOUND ERRORS ARE RECORDED BUT
                ;        NO NAKS ARE SENT.

000006  NSNBF   ;@ NAKS SENT - BUFFER TEMP. UNAVAILABLE         (REASON =  8.)  **
000007  NSHCE   ;@ NAKS SENT - HEADER BCC ERROR         (REASON =  1.)  **
000010  NSDCE   ;@ NAKS SENT - DATA BCC ERROR           (REASON =  2.)  **

000011  RST     ;@ REPS SENT - CUMUL REP SENT.
000012  RRCV    ;@ REPS RCVD - CUMUL REP RCVD.

000013  NRREP   ;# NAKS RCVD - REP RESPONSE             (REASON =  3.)
000014  NRROV   ;# NAKS RCVD - RCV OVERRUN              (REASON =  9.)
000015  NRHFM   ;# NAKS RCVD - MSG HDR FORMAT           (REASON = 17.)
000016  NRMTL   ;# NAKS RCVD - MSG TOO LONG             (REASON = 16.)

000017  NSREP   ;# NAKS SENT - REP RESPONSE             (REASON =  3.)
000020  NSROV   ;# NAKS SENT - RCV OVERRUN              (REASON =  9.)  **
000021  NSHFM   ;# NAKS SENT - MSG HDR FORMAT           (REASON = 17.)  **

000022  XUNDR   ;# XMIT UNDERRUN COUNT.

000023  CFAIL   ;# CALL SET UP FAILURE COUNT.

000024  CTSCNT  ;# CTS FAILURE COUNT.

000025  CDLCNT  ;# CARRIER DETECT LOST COUNT
                ;# (WHILE RECEIVING)

000026  RCVIDL  ;# RECEIVER INACTIVE COUNT.

000027  STRCNT  ;# STREAMING TIME-OUT COUNTER

000030  XMBYT   ;# TOTAL NUMBER OF BYTES TRANSMITTED.
                ;# (INCLUDING RETRANSMISSION, 32 BIT
                ;# COUNTER)
000034  RCBYT   ;# TOTAL OF BYTES RECEIVED. (NOT
                ;# INCLUDING DUPLICATE OR OUT OF
                ;# SEQUENCE, 32 BIT COUNTER)

000040  ICSEL   ;# INCOMPLETE SELECTION COUNTER
000041  NRSEL   ;# NO REPLY TO SELECTION COUNTER
```

Figure 4-2 DMR11 Base Table Layout (Sheet 1 of 4)

```
BASE
TABLE
ADDRESS                          BASE TABLE ALLOCATION

        ;NAME
        ;----
        ;
000042  R       ;$ R    -- HIGHEST MSG SUCCESSFULLY RECEIVED
000043  N       ;$ N    -- HIGHEST MSG TRANSMITTED
000044  A       ;$ A    -- HIGHEST MSG ACKNOWLEDGED
000045  T       ;$ T    -- NEXT MSG TO TRANSMIT
000046  X       ;$ X    -- LAST MSG TO COMPLETE TRANSMISSION
000047  TEMPX   ;$ TEMPX --   CURRENT MSG BEING TRANSMITTED


000050  XEQ     ;$ TRANSMIT END OF QUEUE
000051  XBQ     ;$ TRANSMIT BEGINNING OF QUEUE


000052  REQ     ;$ RECEIVE END OF QUEUE
000053  RBQ     ;$ RECEIVE BEGINNING OF QUEUE


000054  NREAS   ;$ LATEST NAK REASON


000055  PRETIM  ;$ PROGRAMMABLE REP/SELECT-TIMER PRESET VALUE
000056  RSTIM   ;$ ISTRT/ASTRT/REP/SELECT-TIMER  COMPARE LEVEL
000057  TIMER   ;$ ACTIVE TIME COUNTER


000060  TH1L    ;$ THRESHOLD LEVEL - 'NAK' RCVD
000061  TH1     ;$ THRESHOLD COUNT - 'NAK' RCVD

000062  TH2L    ;$ THRESHOLD LEVEL - 'NAK' SEND EXCEPT NO BUF
000063  TH2     ;$ THRESHOLD COUNT - 'NAK' SEND EXCEPT NO BUF

000064  TH3L    ;$ THRESHOLD LEVEL - 'REP' SENT
000065  TH3     ;$ THRESHOLD COUNT - 'REP' SENT

000066  TH4L    ;$ THRESHOLD LEVEL - 'NO-BUF' AVAILABLE
000067  TH4     ;$ THRESHOLD COUNT - 'NO-BUF' AVAILABLE


000070  IM.SP   ;$ IMAGE OF SP.04 (SP.XMS)
                ;$ IMAGE OF SP.05 (SP.RCS)
                ;$ IMAGE OF SP.07 (SP.PST)
                ;$ IMAGE OF SP.10 (SP.XFL)
                ;$ IMAGE OF SP.11 (SP.GBL)
                ;$ IMAGE OF SP.   (SP.RFL)
                ;$ IMAGE OF SP.13 (SP.TFL)
                ;$ IMAGE OF MODEM STATUS REGISTER
```

Figure 4-2 DMR11 Base Table Layout (Sheet 2 of 4)

```
BASE
TABLE
ADDRESS                              BASE TABLE ALLOCATION

         ;NAME
         ;----
         ;
000100   XBF0      ;$ XBF0:  (BSEL 4)
                   ;$        (BSEL 5)
                   ;$        (BSEL 7)
                   ;$        (BSEL 6)

000104   XBF1      ;$ XBF1:  (BSEL 4)
                   ;$        (BSEL 5)
                   ;$        (BSEL 7)
                   ;$        (BSEL 6)

000110   XBF2      ;$ XBF2:  (BSEL 4)
                   ;$        (BSEL 5)
                   ;$        (BSEL 7)
                   ;$        (BSEL 6)

000114   XBF3      ;$ XBF3:  (BSEL 4)
                   ;$        (BSEL 5)
                   ;$        (BSEL 7)
                   ;$        (BSEL 6)

000120   XBF4      ;$ XBF4:  (BSEL 4)
                   ;$        (BSEL 5)
                   ;$        (BSEL 7)
                   ;$        (BSEL 6)

000124   XBF5      ;$ XBF5:  (BSEL 4)
                   ;$        (BSEL 5)
                   ;$        (BSEL 7)
                   ;$        (BSEL 6)

000130   XBF6      ;$ XBF6:  (BSEL 4)
                   ;$        (BSEL 5)
                   ;$        (BSEL 7)
                   ;$        (BSEL 6)

000134   XBF7      ;$ XBF7:  (BSEL 4)
                   ;$        (BSEL 5)
                   ;$        (BSEL 7)
                   ;$        (BSEL 6)
```

Figure 4-2 DMR11 Base Table Layout (Sheet 3 of 4)

```
BASE
TABLE
ADDRESS                                  BASE TABLE ALLOCATION

        ;NAME
        ;-----
        ;
000140  RBF0    ;$ RBF0: (BSEL 4)
                ;$       (BSEL 5)
                ;$       *BSEL 7)
                ;$       (BSEL 6)

000144  RBF1    ;$ RBF1: (BSEL 4)
                ;$       *BSEL 5)
                ;$       (BSEL 7)
                ;$       *BSEL 6)

000150  RBF2    ;$ RBF2: (BSEL 4)
                ;$       (BSEL 5)
                ;$       (BSEL 7)
                ;$       *BSEL 6)

000154  RBF3    ;$ RBF3: (BSEL 4)
                ;$       *BSEL 5)
                ;$       (BSEL 7)
                ;$       *BSEL 6)

000160  RBF4    ;$ RBF4: (BSEL 4)
                ;$       *BSEL 5)
                ;$       (BSEL 7)
                ;$       *BSEL 6)

000164  RBF5    ;$ RBF5: (BSEL 4)
                ;$       *BSEL 5)
                ;$       (BSEL 7)
                ;$       *BSEL 6)

000170  RBF6    ;$ RBF6: (BSEL 4)
                ;$       *BSEL 5)
                ;$       (BSEL 7)
                ;$       *BSEL 6)

000174  RBF7    ;$ RBF7: (BSEL 4)
                ;$       *BSEL 5)
                ;$       (BSEL 7)
                ;$       *BSEL 6)
```

Figure 4-2 DMR11 Base Table Layout (Sheet 4 of 4)

4.6.2 EVDMA Repair Level Diagnostics

This diagnostic performs register and USYRT addressing tests, static bit-interaction and read/write logic tests, basic transmitter and receiver sequencing tests, and static operation in character and bit-stuffing modes tests. This program performs many of the tests in Internal Loopback Mode using the

USYRT maintenance bit and the line unit loopback features. In external loopback mode it uses a turnaround connector. This program is implemented as a separate VAX diagnostic, which runs at Level 3.

4.6.3 EVDCA REV** VAX-11/780 Synchronous Link Level Two Diagnostics

The VAX network diagnostic is intended to provide a means to verify a communications link with VAX-11/780 hardware, and to provide a VAX exerciser for the DUP11, DMC11, DMR11, and future synchronous communications options on a link. The diagnostic runs at Level 2, which will eventually support either VMS or stand-alone operation. The DMC11/DMR11 tests allow operation with internal or external data loopback and will be able to communicate with another VAX-11/780, or a PDP-11 node running Data Communication Link Test-11/780. The PDP-11, DCLT programs will provide Field Service with a standalone tool to be used to maintain communications equipment by providing the test coverage necessary to isolate failures to the computer equipment, the communications line, or the modem. The DMR11 can be run using this diagnostic, in DMC11 compatibility mode only, using the VMS DMC-11 driver. These will all run under the VAX supervisor.

4.6.4 Examination of DMR11 Internal Components

Example 1: Examine DMR11 memory

Procedures	Comments
1. Load 0 SEL 0 (to clear Run bit and stop the microprocessor). Done with "D/W" command to reference "word" rather than a "Longword" deposit.	To specify the DMR address, prefix the floating address with 04004_8 to assemble the 32-bit physical address and then convert to HEX (that is, address 760100_8 becomes 04004760100_8, which is $2013E040_{16}$). This procedure assumes the DMR11 to be installed on UBA 0 of the VAX.
2. Load $10XX_{16}$ to SEL 6 using word command reference.	Microinstruction is loaded into SEL 6 where XX is an eight bit memory address which is loaded into MAR.
3. Load 300_{16} to SEL 0 using word command reference.	Set ROM In and Step μP bits.
4. Load $5A94_{16}$ to SEL 6 using word command reference.	Load microinstruction to SEL 6 to read memory content pointed to by MAR to SEL 4. MAR is incremented.
5. Load 300_{16} to SEL 0 using word command reference.	Set ROM In and STEP μP bits.
6. Examine SEL 4 Low byte for memory content using word command reference.	Low byte of SEL 4 contains content of memory location under examination.
7. Go to step 5 for examination of consecutive memory locations.	

Example 2: Examine DMR11 Scratchpad Registers

Procedures	Comments
1. Load 0 to SEL 0 using word command reference. (See example 1 above for procedure to form register addressing on a VAX.)	To clear Run bit.
2. Load $618X_{16}$ to SEL 6 using word command reference.	SEL 6 is loaded with microinstructions, where X is O-F_6 Scratchpad Register and the content of SP is loaded into the Branch Register.
3. Load 300_{16} to SEL 6 using word command reference.	Set ROM In and Step μP bits.
4. Load 6294_{16} to SEL 6 using word command reference.	Load microinstruction, where content of SPX (from BR) is loaded into SEL 4 low byte.
5. Load SEL 0 with 300_{16} using word command reference.	Set ROM In and Step μP bits.
6. Examine BSEL 4 for content of SPX.	BSEL 4 contains contents of scratchpad X.

Example 3: DMR11 Base Table Dump

Procedure	Comments
	NOTE **The UBA Mapping register must be loaded as follows: Load address 20006804 with 80000001.**
1. Load 23_{16} to BSEL 0 using word command reference.	To perform an RQI for Base I type input.
2. Examine BSEL 0 for bit 7 (RDYI) set.	To indicate the microprocessors release of the port.
3. Load 200_{16} to SEL 4 using word command reference.	Giving base address to microprocessor.
4. Load 0 to SEL 6 using word command reference.	Clearing high order address bits and Resume bit.
5. Load 83_{16} to BSEL 0 using word command reference.	To relinquish port back to microprocessor.
6. Load 22_{16} to BSEL 0 using word command reference.	To force a Halt Function with RQI.
7. Examine BSEL 0 for bit 7 (RDI) set.	To indicate the microprocessors release of the port.
8. Load FF_{16} to SEL 4 & SEL 6 using word command reference.	Force Procedural Error.
9. Load 82_{16} to BSEL 0 using word command reference.	To relinquish port back to microprocessor.
10. Examine 128 memory locations starting at 200_{16} to see Base Table.	To see counters, buffers, and other Base Table data.

APPENDIX A
FLOATING DEVICE ADDRESSES AND VECTORS

A.1 FLOATING DEVICE ADDRESSES

UNIBUS addresses starting at 760010 and continuing through 763776 are designated as floating device addresses (see Figure A-1). These are used as register addresses for communications (and other) devices interfacing with the PDP-11 and VAX-11/780.

NOTE

Some devices are not supported by VAX-11/780, however, the same scheme applies; that is, gaps are provided as appropriate. The convention for assigning these addresses is as follows:

Floating CSR Address Devices

Rank	Option	Decimal Size	Octal Modulus
1	DJ11	4	10
2	DH11	8	20
3	DQ11	4	10
4	DU11	4	10
5	DUP11	4	10
6	LK11A	4	10
7	DMC11/DMR11	4	10
8	DZ11* and DZV11	4	10
9	KMC11	4	10
10	LPP11	4	10
11	VMV21	4	10
12	VMV31	8	20
13	DWR70	4	10
14	RL11 and RLV11	4	10 (extra only)

A gap of 10_8 must be left between the last address of one device type and the first address of the next device type. The first address of the next device type must start on a module 10_8 boundary. The gap of 10_8 must also be left for devices that are not installed but are skipped over in the priority ranking list. Multiple devices of the same type must be assigned contiguous addresses. Reassignment of device types already in the system may be required to make room for additional ones.

* DZ11E and DZ11F are dual DZ11s and are treated by the algorithm as two DZ11s.

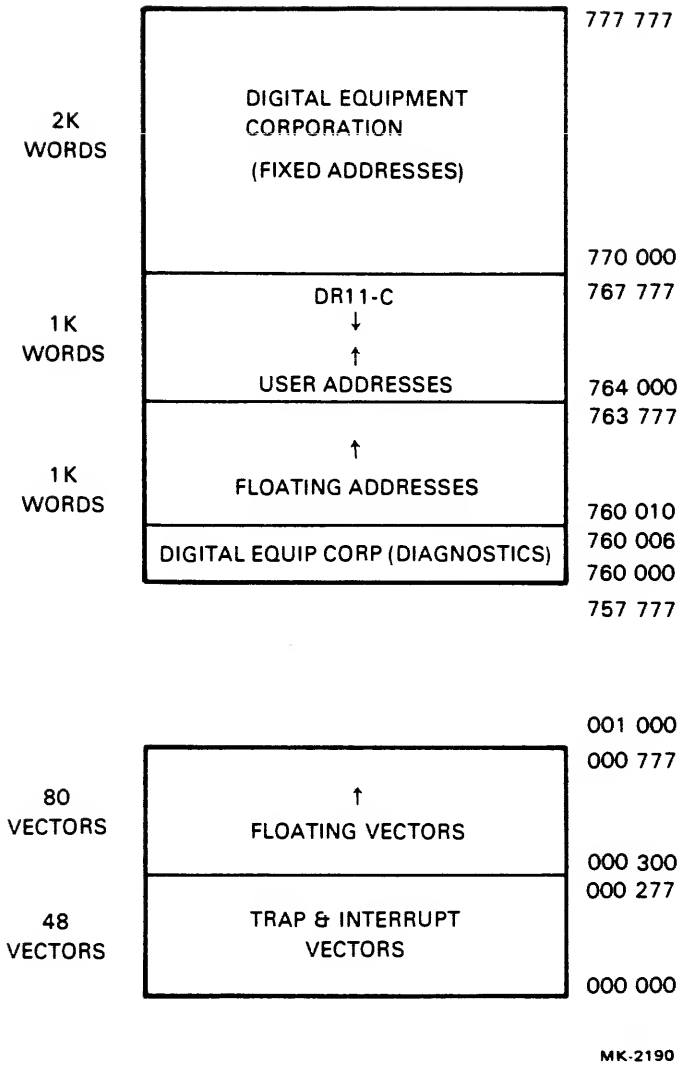


Figure A-1 UNIBUS Address Map

A.2 FLOATING VECTOR ADDRESSES

Vector addresses, starting at 300 and proceeding upward to 777, are designated as floating vectors. These are used for communications (and other) devices that interface with the PDP-11 and VAX-11/780.

NOTE

Some devices are not supported by VAX-11/780, however, the same scheme applies. Vector size is determined by the device type.

There are no gaps in floating vectors unless required by physical hardware restrictions (in data communications devices, the receive vector must be on a zero boundary and the transmit vector must be on a 4_8 boundary).

Multiple devices of the same type would be assigned vectors sequentially. The following chart shows the assignment sequence.

Floating Interrupt Vector Devices

Rank	Option	Decimal Size	Octal Modulus
1	DC11	4	10
2	KL11(extra)	4	10*
2	DL11-A(extra)	4	10*
2	DL11-B(extra)	4	10
3	DP11	4	10
4	DM11-A	4	10*
5	DN11	2	4
6	DM11-BB	2	4
6	DH11 modem control	2	4
7	DR11-A	4	10*
8	DR11-C	4	10*
9	PA611(reader)	2	10*
10	PA611(punch)	2	10*
11	LPD11	4	10
12	DT11	4	10*
13	DX11	4	10*
14	DL11-C	4	10*
14	DL11-D	4	10*
14	DL11-E	4	10*
15	DJ11	4	10*
16	DH11	4	10†
17	GT40	8	10
18	LPS11	12	30*
19	DQ11	4	10†
20	KW11-W	4	10
21	DU11	4	10*
22	DUP11	4	10*
23	DV11	4	10*
24	DV modem control	2	4
25	LK11-A	4	10
26	DWUN	4	10
27	DMC11/DMR11	4	10*
28	DZ11	4	10*
29	KMC11	4	10
30	LPP11	4	10
31	VMV21	4	10
32	VMV31	4	10
33	VTV01	‡	‡
34	DWR70	4	10*
35	RL11/RLV11	2	4
36	RX02	2	4
37	TS11	2	4 (after the first)
38	LPA11-K	4	10
39	IP11/IP300	2	4

* The vector for the device of this type must always be on a 10_8 boundary.

† These devices can have either a M7820 or M7821 interrupt control module. However, it should always be on a 10_8 boundary.

‡ To be determined.

A.3 EXAMPLES OF DEVICE AND VECTOR ADDRESS ASSIGNMENT

Example 1

The first device requiring address assignment in this example is a DH11 (Number two in the device address assignment sequence; Number 16 in the vector address assignment sequence).

The only devices used are:

2 DH11s
2 DQ11s
1 DUP11
1 DMR11

Device (Option)	Device Address	Vector Address	Comment
	760010		Gap left for DJ11 (one on device address assignment sequence) which is not used
DH11	760020	300	First DH11
DH11	760040	310	Second DH11
	760060		Gap between the last DH11 used and the next device
DQ11	760070	320	First DQ11
DQ11	760100	330	Second DQ11
	760110		Gap between the last DQ11 used and the next device
	760120		Gap left for DU11s not used
DUP11	760130	340	Only one DUP11
	760140		Gap left between DUP11 and next device
	760150		Gap left for LK11-As not used
DMR11	760160	350	Only one DMR11
	760170		Gap left after the last device (in this case, the DMR11) to indicate that none follow

Example 2

The only devices used in this example are:

1 DJ11
1 DH11
2 DQ11s
2 DUP11s
2 DMR11s

Device (Option)	Device Address	Vector Address	Comment
DJ11	760010	300	Only one DJ11
	760020		Gap left between DJ11 and the next device
	760030		Gap – The next device, DH11, must start on an address boundary that is a multiple of 20
DH11	760040	310	Only one DH11
	760060		Gap left between DH11 and next device
DQ11	760070	320	First DQ11
DQ11	760100	330	Second DQ11
	760110		Gap left between DQ11 and next device
	760120		Gap left for DU11s not used
DUP11	760130	340	First DUP11
DUP11	760140	350	Second DUP11
	760150		Gap left between the last DUP11 and next device
	760160		Gap left for LK11-As not used
DMR11	760170	360	First DMR11
DMR11	760200	370	Second DMR11
	760210		Gap left after the last device (in this case the DMR11) to indicate that none follow

Example 3

Only one of each of the following devices are used in this example:

DC11
DJ11
DH11
GT40
DQ11
DUP11
DMR11
DMC11

Device (Option)	Device Address	Vector Address	Comment
DC11		300	DC11 has a fixed device address
DJ11	760010	310	Only one DJ11
	760020		Gap left between DJ11 and the next device
	760030		Gap – The next device, DH11, must start on an address boundary that is a multiple of 20
DH11	760040	320	Only one DH11
	760060		Gap left between DH11 and next device
GT40		330	GT40 has a fixed device address
DQ11	760070	340	Only one DQ11
	760100		Gap left between DQ11 and next device
	760110		Gap left for DU11s not used
DUP11	760120	350	Only one DUP11
	760130		Gap left between DUP11 and the next device
	760140		Gap left for LK11-As not used
DMR11	760150	360	Only one DMR11
DMC11	760160	370	Only one DMC11
	760170		Gap left after the last device (DMC11) to indicate that none follow

APPENDIX B
DDCMP IN A NUTSHELL

B.1 DDCMP

DDCMP (DIGITAL Data Communications Message Protocol) was developed to provide full-duplex message transfers over existing standard hardware.

B.1.1 Controlling Data Transfers

The DDCMP message format is shown in Figure B-1. A single control character is used in a DDCMP message and is the first character in the message. Three control characters are provided in DDCMP to differentiate between the three possible types of messages:

SOH – data message follows
ENQ – control message follows
DLE – bootstrap message follows

Note that the use of a fixed-length header and message size declaration obviates the requirement for extensive message and header delimiter codes.

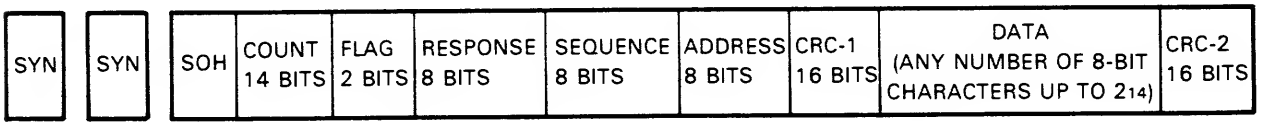


Figure B-1 DDCMP Data Message Format

Figure B-2 shows an example of a data exchange.

B.1.2 Error Checking and Recovery

DDCMP uses a 16-bit cycle redundency check (CRC-16) for detecting transmission errors. When an error occurs, DDCMP sends a separate negative acknowlege (NAK) message. DDCMP does not require an acknowledgement message for all data messages. The number in the response field of a normal header or in either the special NAK or acknowledge (ACK) message specifies the sequence number of the last good message received. For example, if messages 4, 5, and 6 have been received since the last time an acknowledgement was sent and message 6 is bad, the NAK message specifies number 5 which says "messages 4 and 5 are good and 6 is bad." When DDCMP operates in full-duplex mode, the line does not have to be turned around; the NAK is simply added to the sequence of messages for the transmitter.

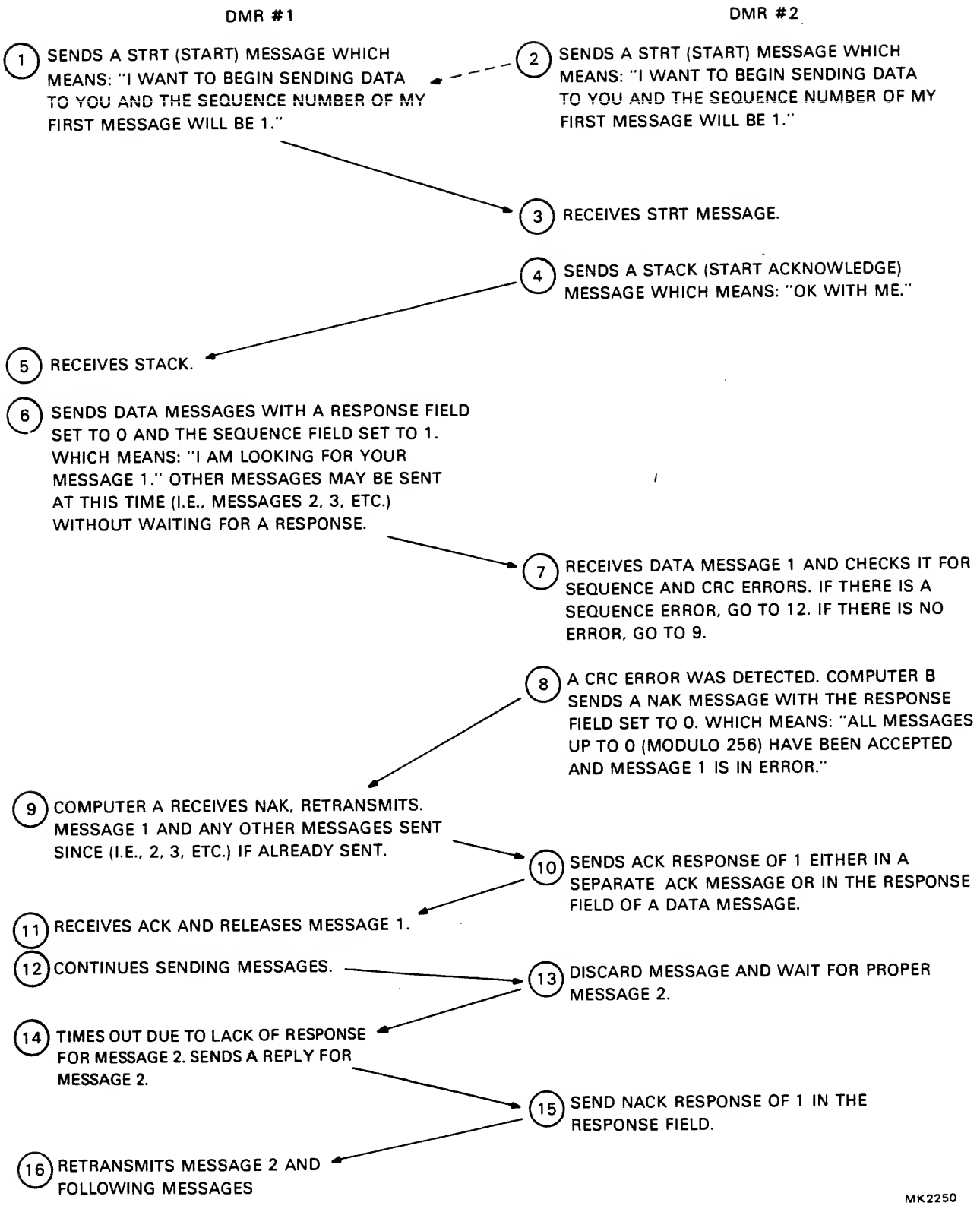


Figure B-2 DDCMP Sample Handshaking Procedure

When a sequence error occurs in DDCMP, the receiving station does not respond to the message. The transmitting station detects, from the response field of the messages it receives (or via timeout), that the receiving station is still looking for a certain message and sends it again. For example, if the next message the receiver expects to receive is 5, but receives 6 instead, the receiver will not change the response field (which contains a 4) of its data messages. The receiver will say, "I accept all messages up through message 4 and I'm still looking for message 5."

B.1.3 Character Coding

DDCMP uses ASCII control characters for SYN, SOH, ENQ and DLE. The remainder of the message, including the header, is transparent.

B.1.4 Data Transparency

DDCMP defines transparency by use of a count field in the header. The header is of a fixed length. The count in the header determines the length of the transparent information field, which can be from 0 to 16,383 bytes long. To validate the header and count field, it is followed by a CRC-16 field; all header characters are included in the CRC calculation. Once validated, the count is used to receive the data and to locate the second CRC-16, which is calculated on the data field. Thus, character stuffing is avoided.

B.1.5 Data Channel Utilization

DDCMP uses either full-duplex or half-duplex circuits at optimum efficiency. In the full-duplex mode, DDCMP operates as two independent one-way channels, each containing its own data stream. The only dependency is the acknowledgements which must be sent in the data stream in the opposite direction.

Separate ACK messages are unnecessary, reducing the control overhead. Acknowledgements are simply placed in the response field of the next message for the opposite direction. If several messages are received correctly before the terminal is able to send a message, all of them can be acknowledged by one response. Only when a transmission error occurs, or when traffic in the opposite direction is light (no data message to send), is it necessary to send a special NAK or ACK message, respectively.

In summary, DDCMP data channel utilization features include:

1. The ability to run on full-duplex or half-duplex data channel facilities,
2. Low control character overhead,
3. No character stuffing,
4. No separate ACKs when traffic is heavy; this saves on extra SYN characters and inter-message gaps,
5. Multiple acknowledgements (up to 255) with one ACK, and
6. The ability to support point-to-point and multipoint lines.

B.2 PROTOCOL DESCRIPTION

DDCMP is a very general protocol; it can be used on synchronous or asynchronous, half-duplex or full-duplex, serial or parallel, and point-to-point or multipoint systems. Most applications involving protocols are half-duplex or full-duplex transmission in a serial synchronous mode; that operating environment will therefore be emphasized in this description.

The header is the most important part of the message because it contains the message sequence numbering information and the character count, the two most important features of DDCMP. Because of the importance of the header information, it merits its own CRC block check, indicated in Figure B-3 as CRC-1. Messages that contain data, rather than just control information, have a second section which contains any number of 8-bit characters (up to a maximum of 16,363) and a second CRC (indicated in Figure B-3 as CRC-2).

Before the message format is discussed in greater detail, the message sequencing system should be explained because most of the header information is directly or indirectly related to the sequencing operation.

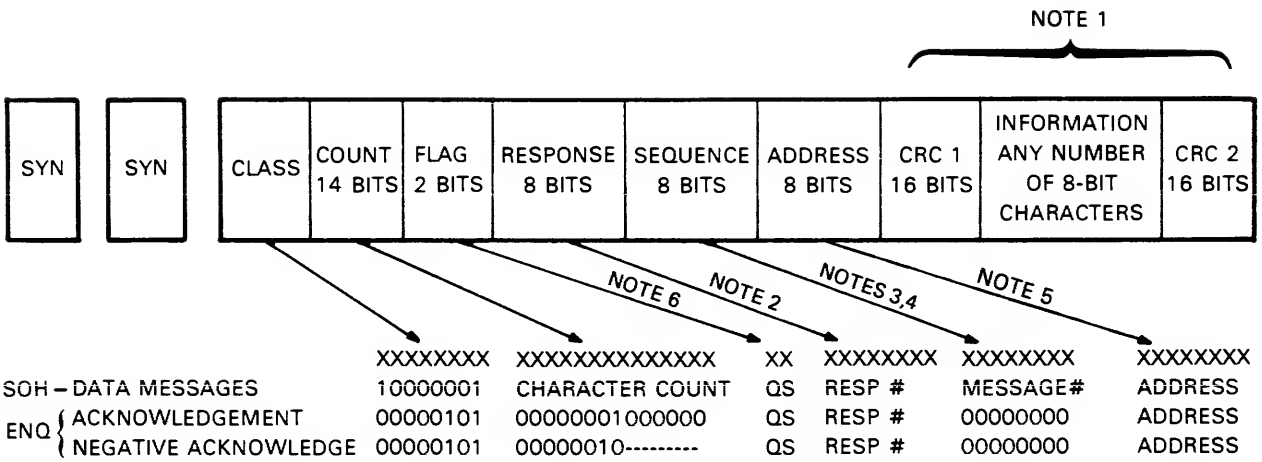
In the DDCMP, any pair of stations that exchange messages with each other number those messages sequentially starting with message number one. Each successive data message is numbered using the next number in sequence, modulo 256. Thus, a long sequence of messages would be numbered 1, 2, 3,...254, 255, 0, 1,... The numbering applies to each direction separately. For example, station A might be sending its messages 6, 7, and 8 to station B, while station B is sending its messages 5, 6, and 7 to station A. Thus, in a multipoint configuration where a control station is engaged in two-way communication with 10 tributary stations, there are 20 different message number sequences involved – one sequence for messages from each of the 10 tributaries to the control station and one sequence for messages from the control station to each of the 10 tributaries.

Whenever a station transmits a message to another station, it assigns its next sequential message number to that message and places that number in the sequence field of the message header. In addition to maintaining a counter for the sequentially numbered messages which it sends, the station also maintains a counter of the message numbers received from the other station. It updates that counter whenever a message is received with a message number exactly one higher than the previously received message number. The contents of the received message counter are included in the response field of the message being sent, to indicate to the other station the highest sequenced message that has been received.

When a station receives a message containing an error, that station sends a negative acknowledge (NAK) message back to the transmitting station. DDCMP does not require an acknowledgement for each message, as the number in the response field of a normal header (or in either the special NAK or positive acknowledgement message ACK), specifies the sequence number of the last good message received. For example, if messages 4, 5, and 6 have been received since the last time an acknowledgement was sent, but message 6 is bad, the NAK message specifies number 5 which says "messages 4 and 5 are good and 6 is bad." When DDCMP operates in the full-duplex mode, the line does not have to be turned around; the NAK is simply added to the messages for the transmitter.

When a station receives a message that is out of sequence, it does not respond to that message. The transmitting station will detect this from the response field of the messages which it receives; if the reply wait timer expires before the transmitting station receives an acknowledgement, the transmitting station will send a REP message. The REP message contains the sequence number of the most recent unacknowledged message sent to the distant station. If the receiving station has correctly received the message referred to in the REP message (as well as the messages preceding it), it replies to the REP by sending an ACK. If it has not received the message referred to in sequence, it sends a NAK containing the number of the last message that it did receive correctly. The transmitting station will then retransmit all data messages after the message specified in the NAK.

The numbering system for DDCMP messages permits up to 255 unacknowledged messages outstanding, a useful feature when working on high delay circuits such as those using satellites.



		XXXXXXXX	XXXXXXXXXXXXXX	XX	XXXXXXXX	XXXXXXXX	XXXXXXXX
SOH – DATA MESSAGES		10000001	CHARACTER COUNT	QS	RESP #	MESSAGE#	ADDRESS
ENQ	ACKNOWLEDGEMENT	00000101	00000001000000	QS	RESP #	00000000	ADDRESS
	NEGATIVE ACKNOWLEDGE	00000101	00000010---------	QS	RESP #	00000000	ADDRESS

REASONS:

BCC HEADER ERROR	000001
BCC DATA ERROR	000010
REP RESPONSE	000011
BUFFER UNAVAILABLE	001000
RECEIVER OVERRUN	001001
MESSAGE TOO LONG	010000
HEADER FORMAT ERROR	010001

ENQ	REPLY MESSAGE	00000101	00000011000000	QS	00000000	LSTMESS#	ADDRESS
	START MESSAGE	00000101	00000110000000	11	00000000	00000000	ADDRESS
	START ACKNOWLEDGEMENT	00000101	00000111000000	11	00000000	00000000	ADDRESS
DLE	MAINTENANCE MESSAGE	10010000	CHARACTER COUNT	11	00000000	00000000	ADDRESS

NOTES:

1. ONLY THE DATA MESSAGE AND THE MAINTENANCE MESSAGE HAVE CHARACTER COUNTS, SO ONLY THESE MESSAGES HAVE THE INFORMATION AND CRC2 FIELDS SHOWN IN THE MESSAGE FORMAT DIAGRAM ABOVE.

2. "RESP #" REFERS TO RESPONSE NUMBER. THIS IS THE NUMBER OF THE LAST MESSAGE RECEIVED CORRECTLY. WHEN USED IN A NEGATIVE ACKNOWLEDGE MESSAGE, IT IS ASSUMED THAT THE NEXT HIGHER NUMBERED MESSAGE WAS NOT RECEIVED, WAS RECEIVED WITH ERRORS, OR WAS UNACCEPTED FOR SOME OTHER REASON. SEE "REASONS."

3. "MESSAGE#" IS THE SEQUENTIALLY ASSIGNED NUMBER OF THIS MESSAGE. NUMBERS ARE ASSIGNED BY THE TRANSMITTING STATION MODULO 256; I.E., MESSAGE 000 FOLLOWS 255.

4. "LSTMESS#" IS THE NUMBER OF THE LAST MESSAGE TRANSMITTED BY THE STATION. SEE THE TEXT DISCUSSION OF REP MESSAGES.

5. " ADDRESS" IS THE ADDRESS OF THE TRIBUTARY STATION IN MULTIPOINT SYSTEMS AND IS USED IN MESSAGES BOTH TO AND FROM THE TRIBUTARY. IN POINT TO POINT OPERATION, A STATION SENDS THE ADDRESS "1" BUT IGNORES THE ADDRESS FIELD ON RECEPTION.

6. "Q" AND "S" REFER TO THE QUICK SYNC FLAG BIT AND THE SELECT BIT. SEE TEXT.

MK-2249

Figure B-3 DDCMP Message Format in Detail

B.3 MESSAGE FORMAT

With the above background, it is now time to explore the various DDCMP message formats in full detail, as shown in Figure B-3. The first character of the message is the class of message indicator, represented in ASCII with even parity. There are three classes of messages: data, control, and maintenance. These are indicated by class of message indicators SOH, ENQ, and DLE respectively. The next two characters of the message are broken into a 14-bit field and a 2-bit field. The 14-bit field is used in data and maintenance messages to indicate the number of characters that will follow the header and form the information part of the message. In control messages, the first 8 bits of the 14-bit field are used to designate what type of control message it is; the last 6 bits are generally filled up with zeros. The exception is in NAK messages where the last six bits are used to specify the reason for the NAK. The 2-bit field contains the quick sync and select flags.

The quick sync flag is used to inform the receiving station that the message will be followed by sync characters; the receiver may wish to set its associated synchronous receiver hardware into sync search mode and sync strip mode. This will re-establish synchronization and syncs will be discarded until the first character of the next message arrives. The purpose of this is to permit the receiving station to engage any hardware sync-stripping logic it might have and prevent it from filling its buffers with sync characters. The select flag is used to indicate that this is the last message which the transmitting station is going to transmit and that the addressed station is now permitted to begin transmitting. This flag is useful in half-duplex or multipoint configurations, where transmitters need to get turned on and off.

The response field contains the number of the last message correctly received. This field is used in data messages and in the positive and negative acknowledge types of control message. Its function should be evident from the preceding discussion of sequence control.

The sequence field is used in data messages and in the REP type of control message. In a data message, it contains the sequence number of the message as assigned by the transmitting station. In a REP message, it is used as part of the question, "Have you received all messages up through message number (specify) correctly?"

The address field is used to identify the tributary station in multipoint systems and is used in messages both to and from the tributary. In point-to-point operation, a station sends address 1, but ignores the address field on reception.

In addition to the positive and negative acknowledgement and REP types of control message, there are also start and start acknowledge control messages. These are used to place the station which receives them in a known state. In particular, they initialize the message counters, timers, and other counters. The start acknowledge message indicates that this has been accomplished.

Figure B-3 also shows the maintenance message. This is typically a bootstrap message containing load programs in the information field. A complete treatment of bootstrap messages and start up procedures is beyond the scope of this book.

NOTE

Refer to the *DDCMP Specification Order* (AA-D599A-TC) for a complete detailed description of DDCMP.

APPENDIX C
DIAGNOSTIC SUPERVISOR SUMMARY

C.1 INTRODUCTION

The PDP-11 diagnostic supervisor is a software package which:

- Provides run-time support for diagnostic programs running on a PDP-11 in Stand-alone Mode,
- Provides a consistent operator interface to load and run a single diagnostic program or a script of programs,
- Provides a common programmer interface for diagnostic development,
- Imposes a common structure upon diagnostic programs,
- Guarantees compatibility with various load systems such as APT, ACT, SLIDE, XXUP+, ABS Loader, and
- Performs non-diagnostic functions for programs, such as console I/O, data conversion, test sequencing, program options.

C.2 VERSIONS OF THE DIAGNOSTIC SUPERVISOR

File Name	Environment
HSAA **.SYS	XXDP+
HSAB **.SYS	APT
HSAC **.SYS	ACT/SLIDE
HSAD **.SYS	Paper Tape (Absolute Loader)

In the above file names, " ** " is for REV and patch level, such as "AO".

C.3 LOADING AND RUNNING A SUPERVISOR DIAGNOSTIC

A supervisor-compatible* diagnostic program may be loaded and started in the normal way, using any of the supported load systems. Using XXDP+ for example, the program "CZDMRB.BIN" is loaded and started by typing .R CZDMRB.

*To determine if diagnostics are supervisor-compatible, use the List command under the Setup Utility (see section C.5.).

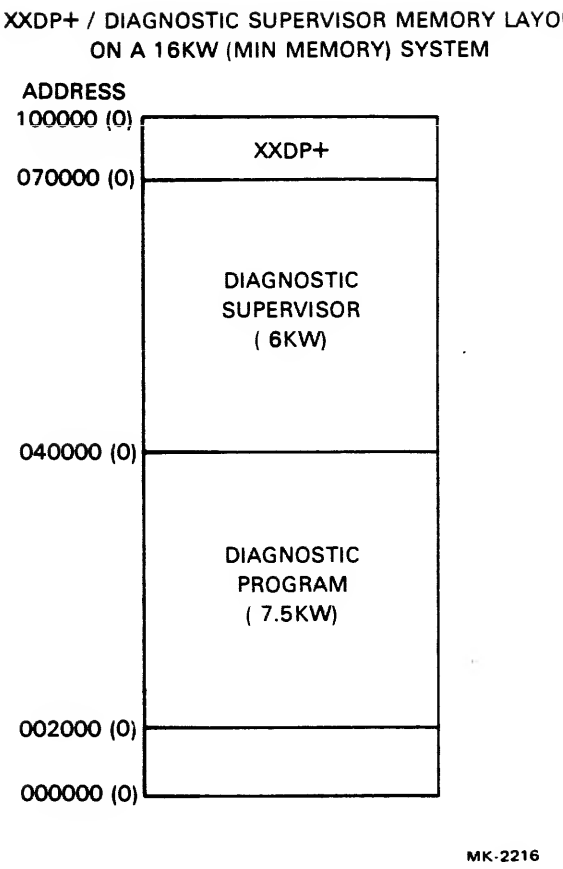


Figure C-1 XXDP+/Diagnostic Supervisor Memory Layout on a 16Kw (Min Memory) System

The diagnostic and the supervisor are automatically loaded to the memory location (as shown in Figure C-1) and the program is started. The following message is typed by the program:

```
DRS LOADED
DIAG.RUN-TIME SERVICES
CZDMR-B-0
M8203 STATIC LOGIC TESTS - PART 1 OF 2
UNIT IS M8203
DR>
```

DR> is the prompt for the diagnostic supervisor routine. At this point a supervisor command must be entered (the supervisor commands are listed in section C.4).

C.3.1 Five Steps to Run a Supervisor Diagnostic

- STEP 1 - Enter start command.

  When the prompt "DR>" is issued, type:

  STA/PASS:1/FLAGS:HOE <CR>

  The switches and flags are optional.

- STEP 2 – Enter number of units to be tested.

  The program will respond to the Start command with:

  # UNITS?

  At this point the number of devices to be tested must be entered.

- STEP 3 – Answer hardware parameter questions.

  After the number of devices to be tested has been entered, the program will respond by asking a number of "Hardware Questions." The answers to these questions are used to build hardware parameter tables in memory. One of these "Hardware P-Tables" will be built for each device to be tested and the series of questions will be posed for each device.

- STEP 4 – Answer software parameter questions.

  When all the "Hardware P-Tables" are built, the program will respond with:

  CHANGE SW?

  If other than the default parameters are desired for the software, type "Y." If the default parameters are desired, type "N."

  If "Y" is typed, a series of "Software Questions" will be asked and the answers to these will be entered into the "Software P-Table" in memory. The software questions will be asked only once, regardless of the number of units to be tested.

- STEP 5 – Diagnostic execution.

  After the software questions have been answered, the diagnostic will begin to run.

  What happens next will be determined by the switch options selected with the Start command, or errors occurring during execution of the diagnostic.

C.4 SUPERVISOR COMMANDS

The supervisor commands that may be issued in response to the "DR>" prompt are as follows:

- Start Command – Used to start a diagnostic program.
- Restart Command – When a diagnostic has stopped and control is given back to the supervisor, this command may be used to restart the program from the beginning.
- Continue Command – Used to allow a diagnostic to continue running from where it was stopped.
- Proceed Command – Causes the diagnostic to resume with the next test after the one in which it halted.
- Exit Command – Transfers control to the XXDP+ monitor.

- Drop Command - Drops units specified until an Add or Start Command is given.
- Add Command - Adds units specified. These units must have been previously dropped.
- Print Command - Prints out statistics if available.
- Display Command - Displays P-Tables.
- Flags Command - Used to change flags.
- ZFLAGS - Clears flags.

All of the supervisor commands except Exit, Print, Flags, and ZFLAGS can be used with switch options.

C.4.1 Command Switches

Switch options may be used with most supervisor commands. The available switches and their function are as follows:

- ./TESTS: - Used to specify the tests to be run (the default is all tests). An example of the tests switch used with the Start command to run tests 1 through 5, 19, and 34 through 38 would be:

  DR> START/TESTS : 1-5 : 19 : 34-38 <CR>

- ./PASS: - Used to specify the number of passes for the diagnostic to run. For example:

  DR> START/PASS : 1

  In this example, the diagnostic would complete one pass and give control back to the supervisor.

- ./EOP: - Used to specify how many passes of the diagnostic will occur before the end of pass message is printed (the default is one).

- ./UNITS: - Used to specify the units to be run. This switch is valid only if "N" was entered in response to "CHANGE HW?"

- ./FLAGS: - Used to check for conditions and modify program execution accordingly. The conditions checked for are:

  :HOE -Halt an error (transfers control back to the supervisor)

  :LOE - Loop on error

  :IER - Inhibit error reports

  :IBE - Inhibit basic error information

  :IXE - Inhibit extended error information

  :PRI - Print errors on line printer

  :PNT - Print the number of the test being executed prior to execution

:BOE – Ring bell on error

:UAM – Run in unattended mode, bypass manual intervention tests

:ISR – Inhibit statistical reports

:IOU – Inhibit dropping of units by program

C.4.2 Control/Escape Characters Supported

The keyboard functions supported by the diagnostic supervisor are as follows:

- CONTROL C (↑C) – Used to return control to the supervisor. The "DR>" prompt would be typed in response to CONTROL C. This function can be typed at any time.
- CONTROL Z (↑Z) – Used during hardware or software dialogue to terminate the dialogue and select default values.
- CONTROL O (↑O) – Used to disable all printouts. This is valid only during a printout.
- CONTROL S (↑S) – Used during a printout to temporarily freeze the printout.
- CONTROL-Q (↑Q) – Used to resume a printout after a CONTROL S.

C.5 WHAT IS THE SETUP UTILITY?

Setup is a utility program that allows the operator to parameterize a supervisor diagnostic prior to execution. This is valid for either XXDP+ or ACT/SLIDE environments. Setup asks the hardware and software questions and builds the P-Tables.

The commands available under Setup are:

List – list supervisor diagnostics
Setup – create P-Tables
Exit – return control to the supervisor

The format for the List command is:

LIST DDN:FILE.EXT

Its function is to type the file name and creation date of the file specified if it is a revision C or later supervisor diagnostic. If no file name is given, all revision C or later supervisor diagnostics will be listed. The default for the device is the system device and wildcards are accepted.

The format for the Setup command is:

SETUP DDN:FILE.EXT=DDN:FILE.EXT

It will read the input file specified and prompt the operator for information to build P-Tables. An output file will be created to run in the environment specified. File names for the output and input files may be the same. The output and input device may be the same. The default for the device is the system device and wildcards are *not* accepted.

APPENDIX D
MICROCODE OVERVIEW

D.1 INTRODUCTION

This section contains an overview of the major functional hardware areas and the microprogram of the DMR11. For detailed descriptions of the hardware components, refer to the list of related documents in Chapter 1. Chapter 3 contains detailed programming descriptions.

D.2 FUNCTIONAL HARDWARE

The basic flow of data and control signals of the DMR11 system is shown in Figure D-1. Some registers and control logic have been omitted for simplicity. Table D-1 contains brief descriptions of the major functional areas.

D.3 DMR11 MICROPROGRAM

The DMR11 microprogram determines the functions that the M8207-RA microprocessor will perform. This program is stored within the control read only memory (CROM) of the M8207-RA. The microinstruction set contains branch and move instructions. Branch instructions perform conditional and unconditional program jumps, and subroutine entry and return. Move instructions provide inter-register and inter-memory transfers and perform logical and arithmetic operations on the transferred data.

D.3.1 Microprogram Message Processing

The microprogram performs four internal processes to implement data transfers between an external source (modem) and the central computer. As shown in the Executive Flow Diagram, Figure D-2, these processes are: transmit, receive, port service, and timer service. Each process operates independently of the other and is time-shared by the microprocessor. Activity levels within a process are called states. A typical flow diagram of microprogram message processing is shown in Figure D-3. Two examples of message processing are shown in the figure (solid lines and dotted lines).

In the first example, the microprogram flow starts at state XM.A of a transmit process. When the activity within this state is completed, the program proceeds to the receive process at state RCV.A. During the receive process a determination is made as to what action is required (see Figure D-2). In this example, nothing was done in the receive process and the program sequences through a time-service routine if the program clock time-out occurs.

When the timer service state (T.1) has been completed, the program returns to the transmit process. This cycle of activity repeats until the message has been processed completely. Although the processing cycle requires the flow to sequence through each process, there may be state levels entered where no action will take place.

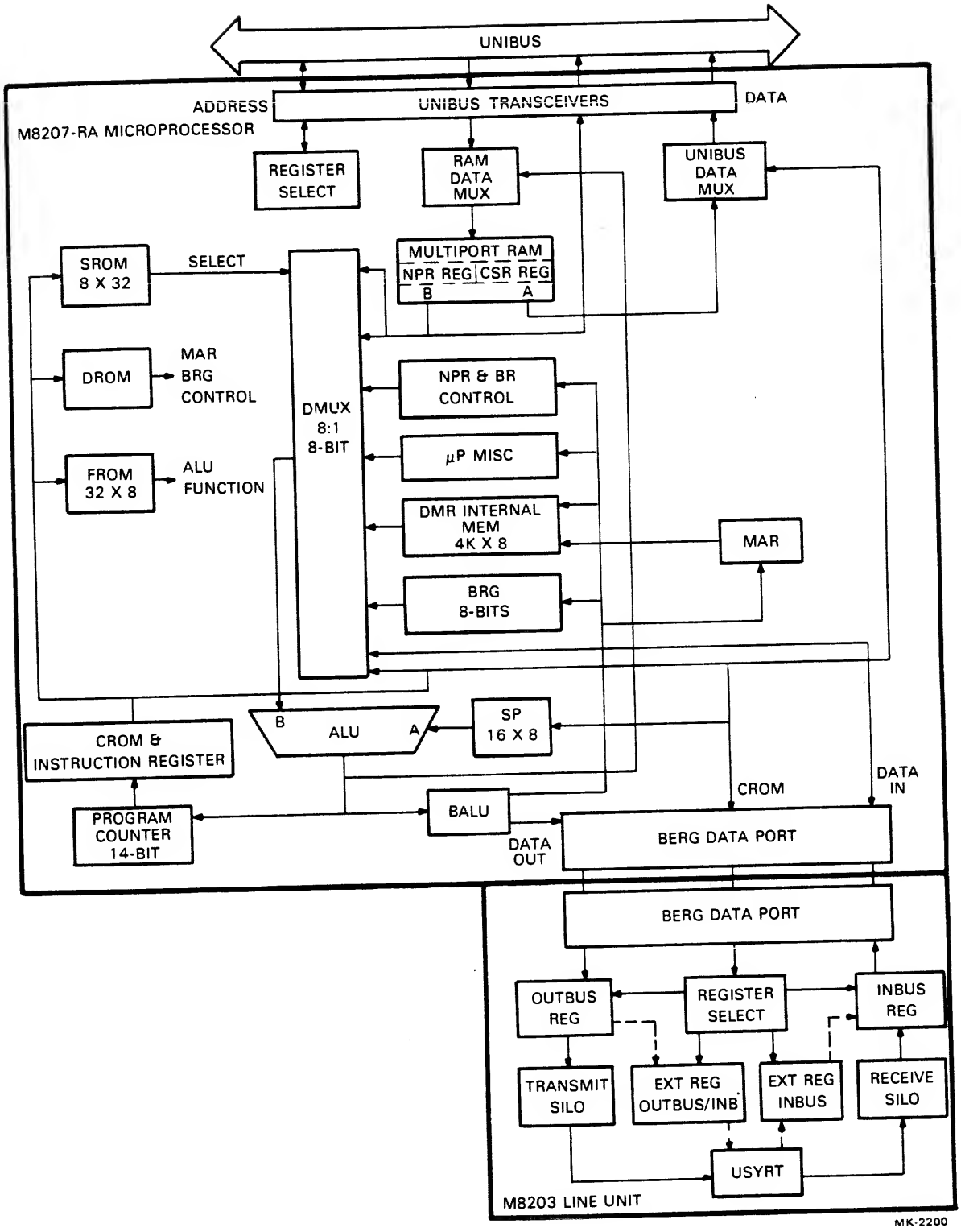


Figure D-1 Data and Control Flow – Basic

Table D-1 Major Functional Areas

Function	Description
ALU Arithmetic Logic Unit	Performs the microprocessor arithmetic and logic operations.
BRG Branch Register	Temporary 8-bit data register for branch determination and rotate right operations. There are three operating modes: load, shift right, and hold.
CROM Control Read Only Memory	Instruction memory. Contains the microprogram (2K, 4K, or 6K × 16-bit).
DMUX Data Multiplexer	8-bit line multiplexer: 8 to 1
DROM Destination ROM	Controls the destination location of data in a move instruction.
FROM	Controls up to 16 functions to be performed by the ALU (32 × 8 bits).
INBUS Input Bus Register	Reads incoming data and status into the receive silo (8-bit register).
IR Instruction Register	Output register of the CROM.
MAR Memory Address Register	Set up by microprocessor to address MEM.
MEM Main Memory	
MIR Maintenance Instruction Register	Used for loading a single microinstruction from the CPU and providing various maintenance functions. Outputs are wire-ORed with IR outputs.
MP RAM Multipart Random Access Memory	Contains the control and status registers that are accessible both internally and by the CPU program. Also contains NPR IN/OUT address and data registers.
NPR Nonprocessor Request and Control	Allows microprocessor to initiate an NPR under microprogram control and gain the UNIBUS to transfer data to or from the CPU memory.
PC Program Counter	Provides the addressing for the CROM. PC control is derived from branch and move instructions.

Table D-1 Major Functional Areas (Cont)

Function	Description
REGISTER SELECT	Decodes selected register address and type of UNIBUS operation requested.
SILO Transmit or Receive	First in, first out register. Receive silo is loaded from the USYRT, transmit silo in the microprocessor (64 × 12).
SP Scratch Pad Memory	Temporary storage register for data (16 × 8 bits).
SROM Source Read Only Memory	Controls input selection for the DMUX. Also determines if a move instruction is to be executed (32 × 8 bits)
System Clock	Provides clock pulses for the microprocessor.
USYRT Universal Synchronous Receiver/Transmitter	Handles input or output data to the modem, and the basic protocol framing and error detection.

The second example (dotted flow lines) shows that the program flow can enter successive process states at any state level. However, it must go through a defined sequence within each process during the cycle.

D.3.2 Transmit Process

Figure D-4 is a macroflow diagram of the transmit process. Areas within the dotted lines indicate microprogram state levels of the message processing cycle (see Figure D-3). Designations in the flow paths are actual program names and may be referred to in the microcode listing and the detailed flow charts included in the engineering print set.

When a message is ready to be sent, the transmitter must determine whether transmission is possible or not. If transmission is possible, the program determines the type of message to be sent and sets up the proper subroutines to process it. Message types, in order of priority, include: negative acknowledge (NAK), reply (REP), data, and acknowledge (ACK).

When the transmitter is ready to send, all the sync signals are transmitted. The program enters the appropriate subroutine to set up the header of the specified message by selecting the type field, subtype field, message field, and response field. It then sets the selection flag in the header storage location, and sends the header out.

If a REP, Start, or Stack message is in progress, the program resets the reply timer and if there is no data to be transmitted, continues toward the shutdown state.

When a data message is being transmitted, the program initiates the first non-processor request (NPR) right after transmitting the header CRC (block check character).

D.3.3 Receive Process

When the microprogram is at the start of the receive process, it is expecting to receive a message. At this point, the program is either in the idle state or prepared to receive messages (see Figure D-5). If it is idle, an attempt is made to update the Base Table. If not, it determines what type of message is being received.

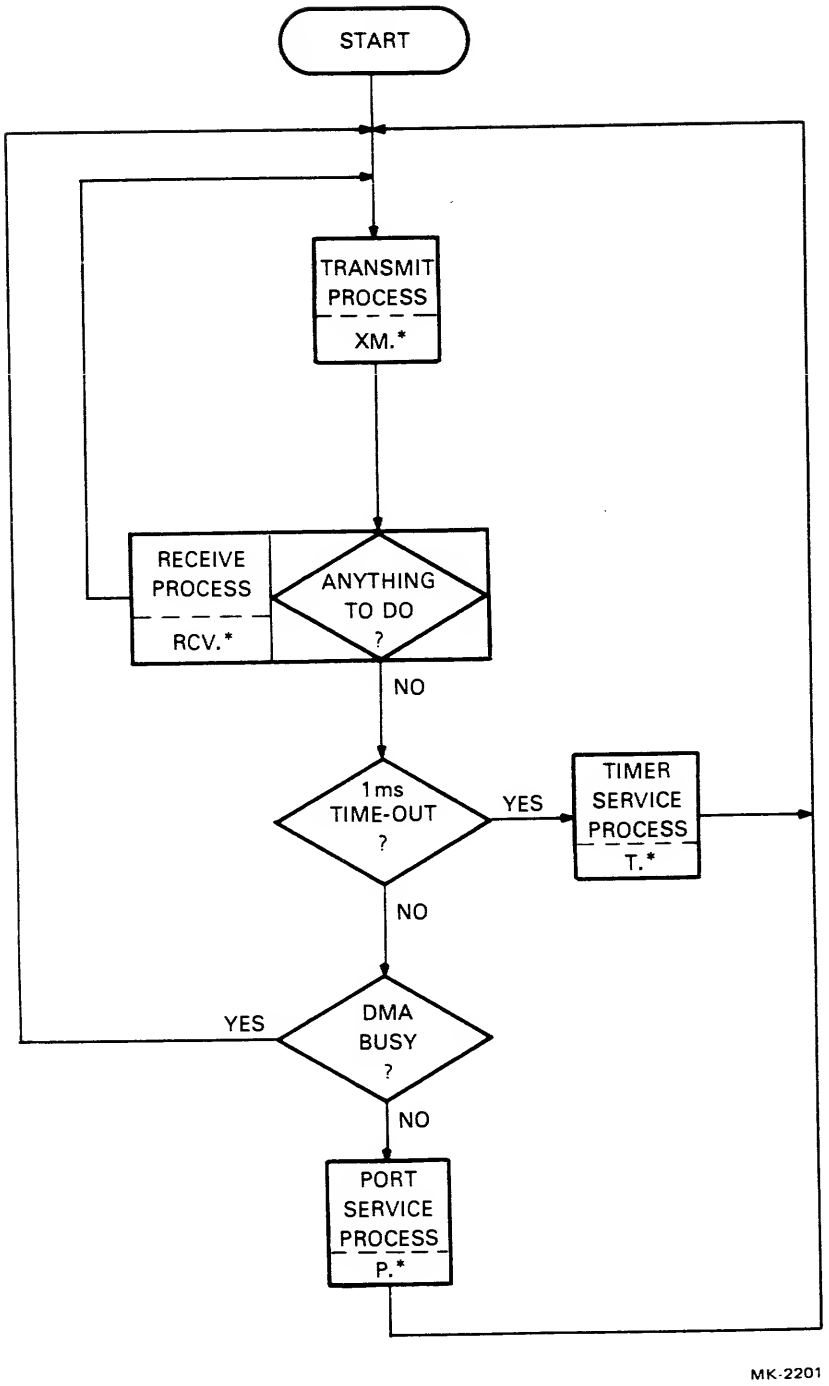


Figure D-2 Executive Flow Diagram

Data fetched from the host memory via NPRs are transmitted on the serial line, followed immediately by CRCs.

The program stores the bytes that make up the header and performs error checking. When an error is detected, a negative acknowledge (NAK) is scheduled and the receiver is cleared, returning it to the idle state. After header storage has been completed, the program sequences through a header verification routine.

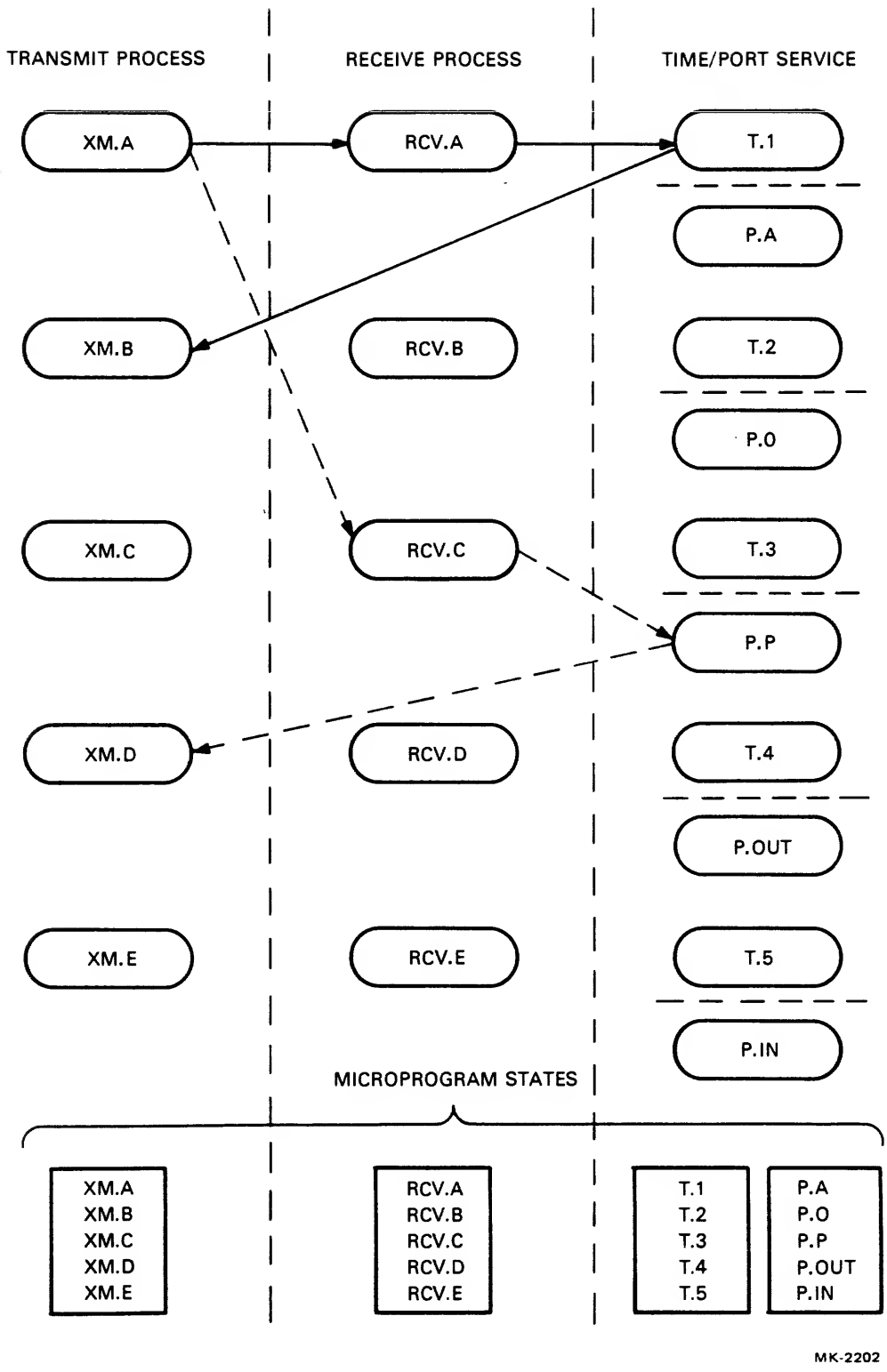


Figure D-3 Typical DMR11 Message Processing

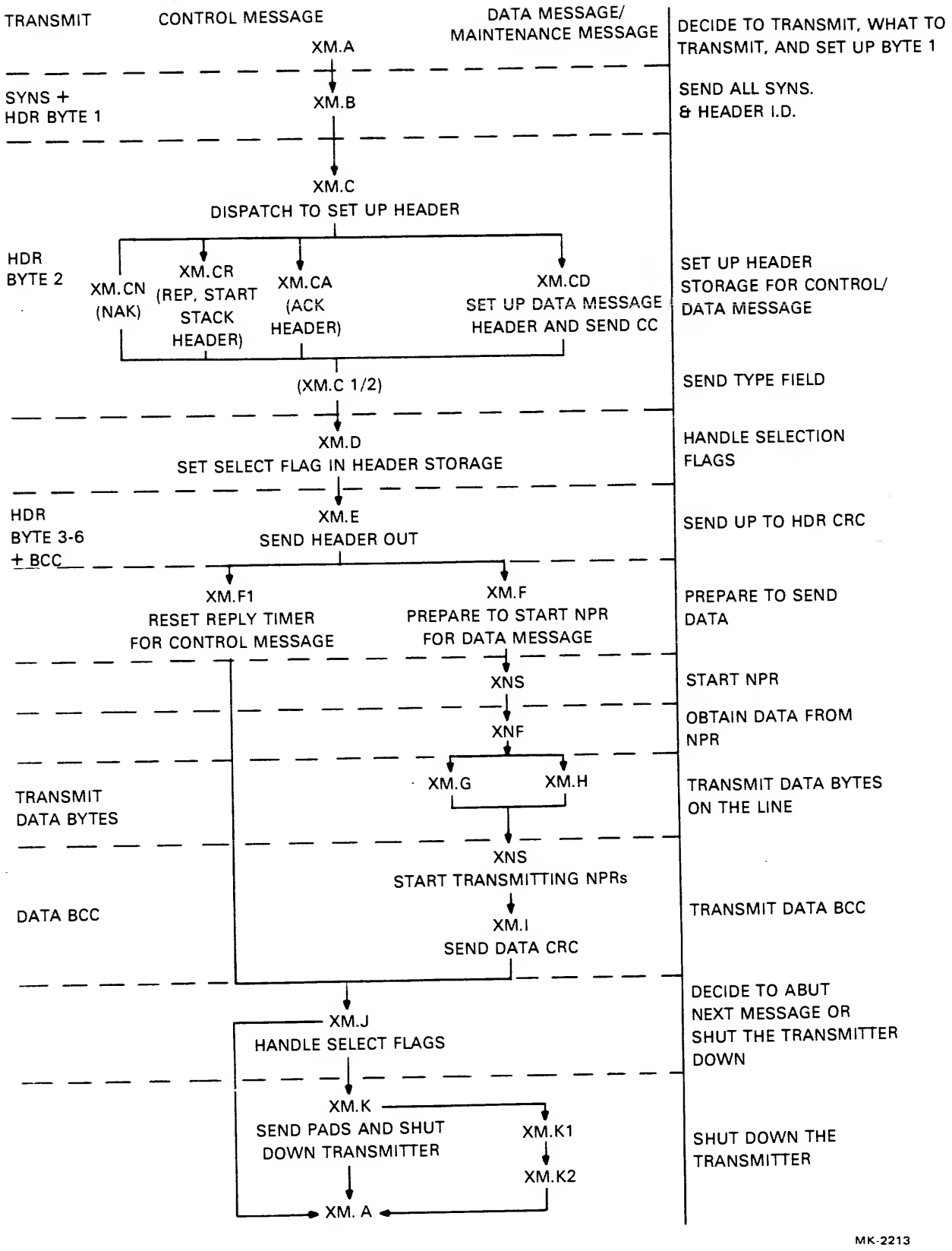


Figure D-4 Transmit Process Flow Diagram

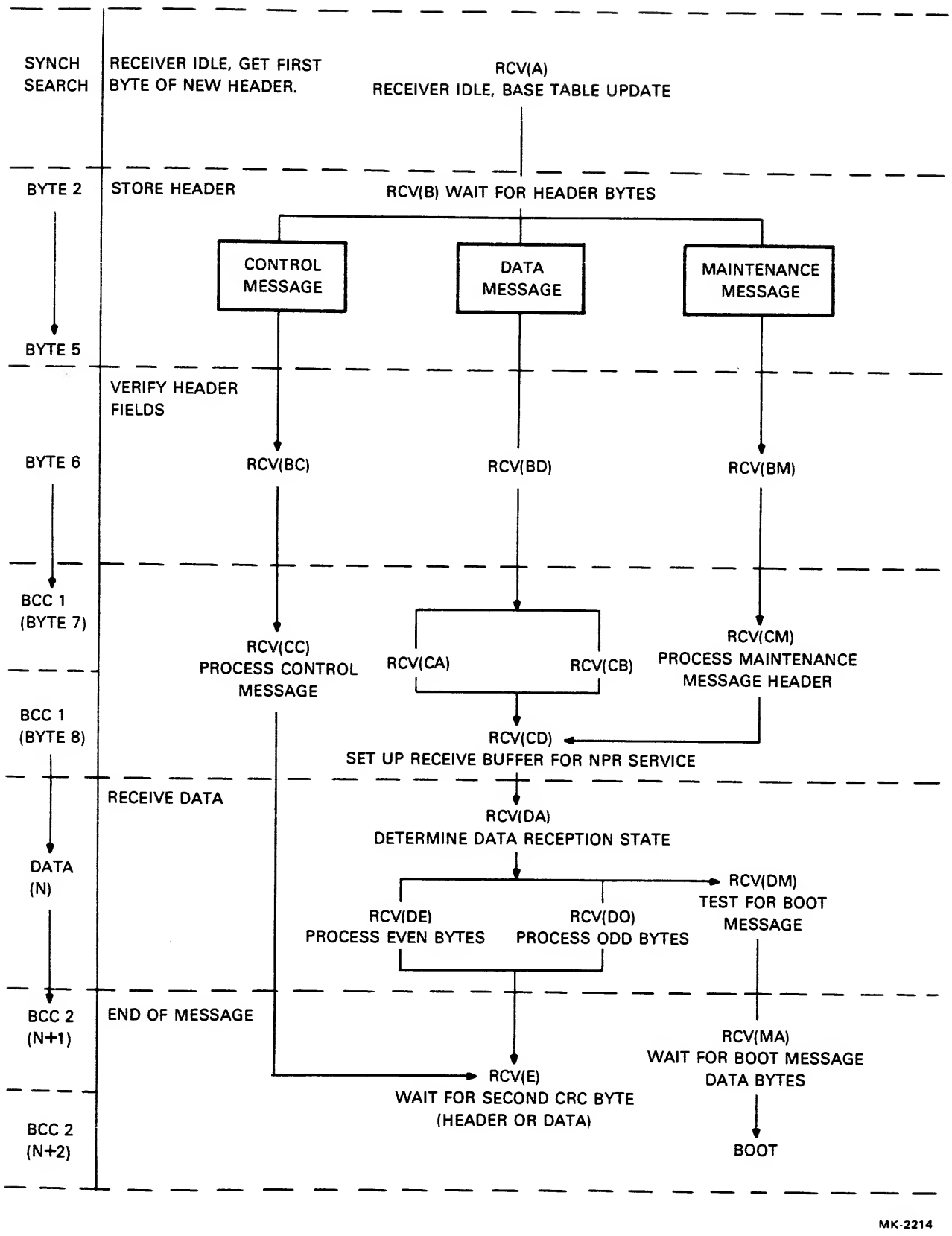


Figure D-5 Receive Process Flow Diagram

The program then performs the specified operation contained in the message. For a control type message, once the operation is complete, the program sequences to the end of message state. For data messages, the implied acknowledge field is processed. If the header is contained in a data message and there is a receive data buffer for storing the incoming data, the DMR11 sets up the buffer for NPR service.

When the incoming message is data, appropriate receiver registers are set up to accept the data from the communication line. The program initiates NPRs to transfer the data to the CPU memory (receive buffers). End of message processing is then performed where checks are made for overrun conditions, block check characters (BCC), and non-existant memory (NXM). After the data has been received and processed properly, the receive buffers are turned to the driver.

If the incoming data is a boot message, control is transferred to a boot message subroutine to process the incoming boot data bytes. A boot password check is made to determine if the message is an Enter MOP (for remote load detect).

APPENDIX E
BOOTSTRAP TEST UNDER ITEP

Interprocessor test programs DZITA* ITEP monitor and DZDMO* ITEP DMC11/DMR11 overlay, provide the capabilities to check out the communications link and to test the ability of the DMR11 to perform both remote load detect and down-line load.

E.1 REMOTE LOAD DETECT

Remote load detect (RLD) is also referred to as unattended system control in Maintenance Operation (MOP) Mode specifications (AA-D60ZA-TC). Unattended system control is defined as follows.

The Enter MOP Mode message is used to control an unattended system. This message, together with the appropriate hardware, enables a satellite computer to halt current operation and begin operating in either the MOP primary or secondary mode. This is accomplished by transferring control to a resident MOP program or bootstrap. The hardware is used to recognize this message and force the computer system to transfer control to the MOP program, usually residing in a read only memory. The password in this message protects the system from being controlled and loaded by an unauthorized host. Only messages with a matching password will cause the system to enter MOP mode.

E.2 DMR11 SETUP FOR REMOTE LOAD DETECT

E.2.1 DMR11 Addressing

When using the DMR11 with a bootstrap module (M9301-YJ or M9312), the DMR11 must be addressed according to the rules for floating address assignment. These rules are outlined in the installation section of this manual. If the address is not set correctly, the module will not find the DMR11 and neither manual booting of the DMR11 nor an RLD works.

E.2.2 DMR11 Line Unit Set up

The DMR11 line unit (M8203), Switch Packs E134 and E121, must be properly set when DMR11 is to be used with a bootstrap module such as the M9301-YJ or M9312. This combination is used in applications where RLD and subsequent down line loading are required.

The set-up of Switch Packs E134 and E121 is only required at the end of the link (satellite station) where the boot module is installed.

Switch Pack E134 (M8203) is configured to contain the 8-bit password specified by the operating system.

- Switch 1 is the LSB, switch 8 is the MSB
- Set switches OFF for a 1
- All switches OFF (SP2=377) inhibits RLD operation

Switch Pack E121 (M8203) is configured to the low order 8 bits of the bootstrap entry point (offset).

- Switch 1 is the LSB, switch 8 is the MSB

NOTE

Switch 1 represents bit 0 of the boot address and should be set to 0.

- Set switches OFF for a 1
- Setting for current M9301-YJ code should be 356 (octal) for booting unit 0 and 374 (octal) for booting unit 1

NOTE

The bootstrap entry point (offset) may be different for bootstrap ROM modules other than the M9301-YJ.

E.3 PROCEDURE TO TEST REMOTE LOAD DETECT UNDER ITEP

Down-line load should not be attemped unless the DMR11 link has been checked out successfully using the link test under DMR11 ITEP. The following switch settings are required on the M9301-YJ and DMR11 line unit (M8203) when using ITEP.

NOTE

The M9301-YJ must have both the power-up boot and diagnostics disabled.

Module/Switch	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	SW9	SW10
Switch Pack E134	ON	ON	ON	ON	ON	ON	ON	ON		
Switch Pack E121	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF		

In this mode, the originating station (the one running ITEP) will send an Enter MOP message to the boot station (the one with M9301-YJ) and initiate a down-line load. Successfully down-line loaded, the boot station will print out a boot complete message. See events for RLD under ITEP which follow the set-up requirements below.

1. Set the Enable/Halt switch on the console of the boot station to the enable position. If the boot station is a PDP-11/34 or PDP-11/04, press INIT (followed by CNTL Halt when using KY11-LB).
2. Under ITEP at the originating station:
   - Modify parameter one to 400,
   - Modify paramter two to 0,
   - Deposit 1004 to console switch register, and
   - Type <CR>.

   The automatic mode Bootstrap test should then complete and print out end pass message.

Events for RLD Under ITEP (See Figure E-1)

1. At CPU one, ITEP steps up DMR11, then assigns Enter MOP Mode (MOP6)

2. a. At CPU two, DMR11 compares MOP6 message received to password setup in line unit Switch Pack at E134.

   b. If all passwords match, DMR11 two writes 173000 plus the contents of Switch Pack at E121 on line unit to location 24, clears location 26, and asserts AC LO on the UNIBUS.

NOTE

Load 125252 into locations 24 and 26. These two locations should be modified if 2b is occuring.

Scope AC LO on CPU two to see if it is pulsing because 2b is occuring.

   c. CPU two program control is transferred to DMR11 boot code in the ROM boot (M9301-YJ type). The correct entry into boot code must be set up in line unit Switch Pack at E121 which contains offset added to 17300.

   d. The DMR11 boot code sets up the DMR11 and sends a Request Secondary Boot (MOP8) message.

3. At CPU one, ITEP checks receipt of MOP8 message and transmits a memory load with transfer address (MOP0) message.

4 a. At CPU two, ROM boot receives MOP0 and transfers program control to location 6.

   b. The down-line loaded program is then executed and a boot complete message is printed at the console terminal.

NOTE

1. **The above procedure will set the password for down-line load to 0. This password is determined by the switch E134 settings on M8203 at the boot station or remote station. When doing down-line load with software, the password used by software must match the password selected on the DMR11 line unit at the remote station; in this case the password is 0.**

2. **For automatic boot (RLD) on successful recognition of the Enter MOP message the remote DMR11 will NPR PC and PS to locations 24 and 26 respectively and then it will assert AC LO. Switch at E121 in the events sequence sets the Bootstrap entry point (offset) to 356 for booting DMR11 unit 0.**

3. **On PDP-11/40, 45, and 70, the AC LO asserted by the DMR11 will cause the CPU to assert DC LO. The setting of M9301-YJ SW2 to OFF, prevents the M9301 from attempting to take control of the address bits during the simulated power-up.**

4. **In order to verify switches at E134 and E121 on the line unit, run any DMR11 diagnostics. The STAT2 under the Map of DMR11 Status will give the actual setup of the switches.**

   STAT2: Low byte (bits 7-0) = E134 (PASSWORD)
   High byte (bits 15-8) = E121 (BOOT OFFSET)

E.4 PROCEDURE TO TEST DOWN-LINE LOAD UNDER ITEP

The down-line load should not be attempted unless the DMR11 link has been checked out successfully, using the link test under DMR11 ITEP.

In this mode, the operator at the boot station has to do a boot to M9301-YJ at the entry point for DMR11 Boot code which sends a request secondary boot message to the originating station (see Figure E-2).

The originating station running ITEP in bootstrap mode then replies with a memory load with transfer address message.

The boot station executes that program and prints out a boot complete message.

Procedure:

1. Under ITEP at the originating station:
   a. Modify parameter one to 2400,
   b. Modify parameter two to 0,
   c. Deposit 1004 in the console switch register, and
   d. Type <CR>.
2. At the boot station, boot the M9301-YJ via one of the following methods:
   a. Type XM under the console emulator,
   b. Load address 7773356 and start, or
   c. On the PDP-11/04 and PDP-11/34, when switch setting on the M9301-YJ is set up to boot the DMR11, a control boot to KY11-LB initiates the boot to the DMR11. This may take two control boots to occur with KY11-LC (CNTRL BOOT/CNTRL HALT/CNTRL BOOT).

NOTE

Refer to the M9301-YJ manual for proper switch setting in each case.

Upon successful completion of a down-line load, the terminal at the boot station prints out a boot complete message.

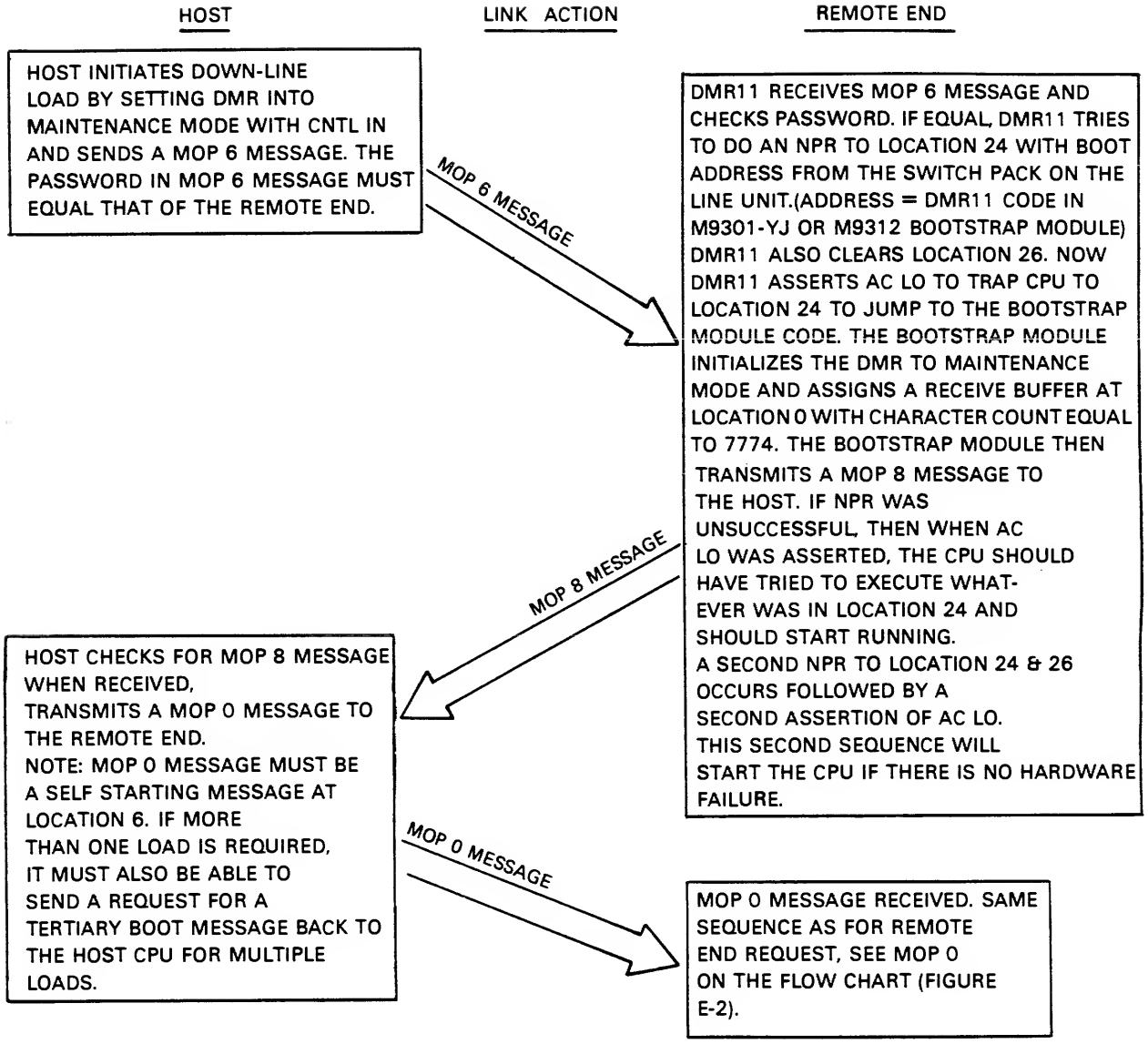


Figure E-1 Down-Line Load to Remote End Using Remote Load Detect

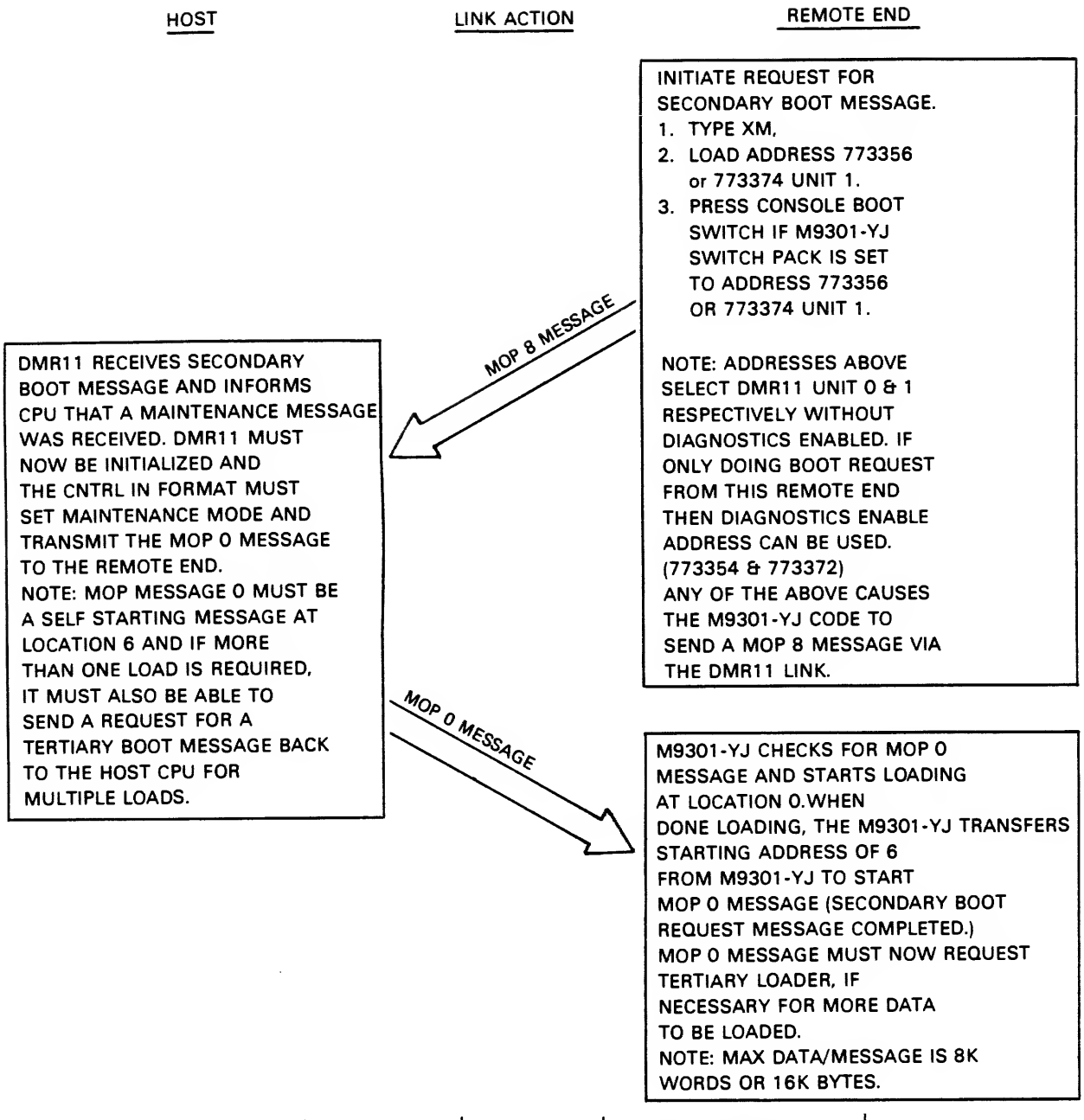


Figure E-2 Remote End Request for Down-Line Load

GLOSSARY

ACKNOWLEDGE (ACK):
Indicates that the previous transmission block was accepted by the receiver and it is ready to accept the next block of the transmission.

ARITHMETIC LOGIC UNIT (ALU):
Allows the microprocessor to perform arithmetic and logic operations.

A PORT:
Read/write input to the multiport RAM.

ASYNCHRONOUS TRANSMISSION:
Transmission in which time intervals between transmitted characters may be of unequal length. Transmission is controlled by start and stop elements at the beginning and end of each character. Also called Start-Stop transmission.

BUFFERED ARITHMETIC LOGIC UNIT (BALU):
Operations performed by the ALU are buffered by the BALU and directed to data memory, respective registers, and the Berg Port.

BERG PORT:
An 8-bit port that allows the microprocessor to communicate with other devices without using the UNIBUS.

BIT-STUFF PROTOCOL:
Zero insertion by the transmitter after any succession of five continuous ones designed for bit-oriented protocols such as IBM's Synchronous Data Link Control (SDLC).

BITS PER SECOND:
Bit transfer rate per unit of time.

B PORT:
Read Address input of the multiport RAM (Read Only Port).

BRANCH REGISTER (BRG):
Temporary card storage register used for branch determination and shifting right.

BUFFER:
Storage device used to compensate for a difference in the rate of data flow when transmitting data from one device to another.

CCITT:
Comite Consultatif Internationale de Telegraphie et Telephonie – An international consultative committee that sets international communications usage standards.

CONTROL AND STATUS REGISTERS (CSRs):
Communication of control and status information is accomplished through these registers.

CRC (CYCLIC REDUNDANCY CHECK):
An error scheme in which the check character is generated by taking the remainder after dividing all the serialized bits in a block of data by a predefined number.

CROM:
Plug-in control read only memory used as the instruction memory for the processor.

CYCLIC REDUNDANCY CHECK (CRC):
An error detection scheme in which the check character is generated by taking the remainder after dividing all the serialized bits in a block of data by a predetermined binary number.

DATA LINK ESCAPE (DLE):
A control character used exclusively to provide supplementary line control signals (control character sequences or DLE sequences). These are two-character sequences where the first character is DLE. The second character varies according to the function desired and the code used.

DATA MULTIPLEXER (DMUX):
An 8-bit wide, 8-to-1 multiplexer used to select data for the B input of the ALU.

DATA-PHONE DIGITAL SERVICE (DDS):
A communications service of the Bell System in which data is transmitted in digital rather than analog form, thus eliminating the need for modems.

DESTINATION ROM (DROM):
Controls the operand as defined by the destination of the instruction in the instruction register.

DIGITAL DATA COMMUNICATIONS PROTOCOL (DDCMP):
DIGITAL's standard communications protocol for character oriented protocol.

DIRECT MEMORY ACCESS (DMA):
Permits I/O transfers directly into or out of memory without passing through the processor's general registers.

ELECTRONIC INDUSTRIES ASSOCIATION (EIA):
A standards organization specializing in the electrical and functional characteristics of interface equipment.

FROM:
Function ROM – Controls up to 16 functions performed by the ALU.

FULL-DUPLEX (FDX):
Simultaneous two-way independent transmission in both directions.

FIELD REPLACEABLE UNIT (FRU):
Refers to a faulty unit not to be repaired in the field. Unit is replaced with a good unit and the faulty unit is returned to a predetermined location for repair.

FIFO:
First In/First Out characteristic of the silo hardware buffer.

HALF-DUPLEX (HDX):
An alternate, one-way-at-a-time independent transmission.

IBUS/OBUS:
Microprocessor NPR control, miscellaneous registers, and CSRs.

IBUS*/OBUS*:
Microprocessor NPR control, miscellaneous registers, and CSRs.

INSTRUCTION REGISTER (IR):
Contains the instruction that is being executed. Outputs are used to control the microprocessor.

LINK MANAGEMENT:
The link management component resolves the transmission and reception on links that are connected to two or more transmitters and/or receivers in a given direction.

LU IBUS:
The line unit input data bus provides a path to the DMUX via the berg connector.

MEMORY ADDRESS REGISTER (MAR):
Controls the data memory for buffered arithmetic and logic operations to main memory.

MAIN MEMORY (MEM):
Data storage area for the microprocessor 4K × 8 RAM; cannot be accessed directly by the CPU.

MAINTENANCE INSTRUCTION REGISTER (MIR):
Provides a destination for an instruction that can be loaded by the CPU during maintenance.

MOP:
Maintenance operation protocol.

MULTIPORT RAM:
Contains all M8207 control and status registers between the microprocessor and the CPU processor.

NEGATIVE ACKNOWLEDGMENT (NAK):
Indicates that the previous transmission block was in error and that the receiver is ready to accept a retransmission of the erroneous block (also a Not Ready Reply to a station selection in multiport).

NON-PROCESSOR REQUEST (NPR):
Direct memory access type transfers, see DMA.

PROGRAM COUNTER (PC):
A 14-bit counter used to control the address of the control ROM directly. PC is derived from Branch and Move instructions.

PROTOCOL:
A formal set of conventions governing the format and relative timing of message exchange between two communicating processes.

RANDOM ACCESS MEMORY (RAM)

READ ONLY MEMORY (ROM)

RS232-C:
EIA standard single-ended interface levels to modem.

RS-422-A:
EIA standard differential interface levels to modem.

RS-423-A:
EIA standard single-ended interface levels to modem.

RS-449:
EIA standard connections for RS-422-A and RS-423-A to modem interface.

SILO:
First in, first out register. Receive silo is loaded from the USYRT, transmit silo from the microprocessor (64 × 12).

SCRATCHPAD MEMORY (SP):
Read/write memory used for temporary storage of data (16 × 8 bits).

SCROM:
Source ROM – Controls input selection for the DMUX. Also determines if a move instruction is to be executed (32 × 8 bits).

SYNCHRONOUS TRANSMISSION:
Transmission in which the data characters and bits are transmitted at a fixed rate with the transmitter and receiver synchronized.

SYSTEM CLOCK:
Basic timing providing clock pulses for microprocessor timing functions.

UNIBUS:
A single high speed bus on which system components connect and communicate with each other. Addresses, data, and control information are transmitted via 56 available lines of the bus.

USYRT:
Universal Synchronous Receiver/Transmitter – Handles input or output data to the modem, and the basic protocol framing and error detection.

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